



# MS-7501 VER:20

## CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

## System Chipset:

AMD/ATI RS780

AMD/ATI SB700

## On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C/RTL8101E

HD Codec -- ALC888

BIOS -- SPI ROM 8M

1394 -- JMB381

## Main Memory:

DDR II X 4 (Max 8GB)

## Expansion Slots:

PCI-E X 16 \*1

PCI-E X 1 \*1

PCI 2.2 Slot X 2

## Clock Generator:

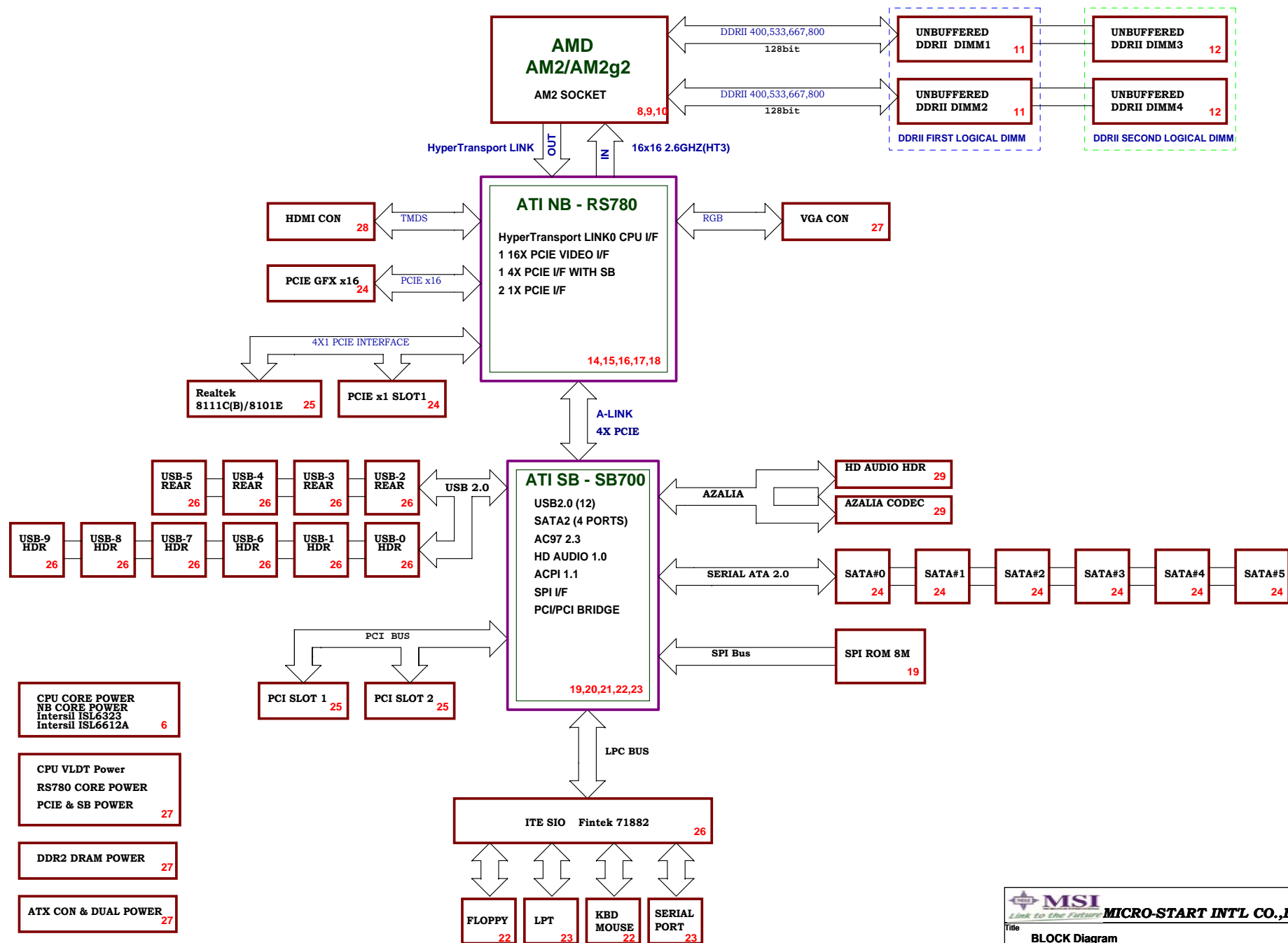
Controller--ICS9LPRS477

## PWM:

Controller -- ST6740L + UP6262 3+1 Phase

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# Project RS-780 BLOCK DIAGRAM



## SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTENTVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SM#/#EXTENTVNT1#		LPC_SM#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

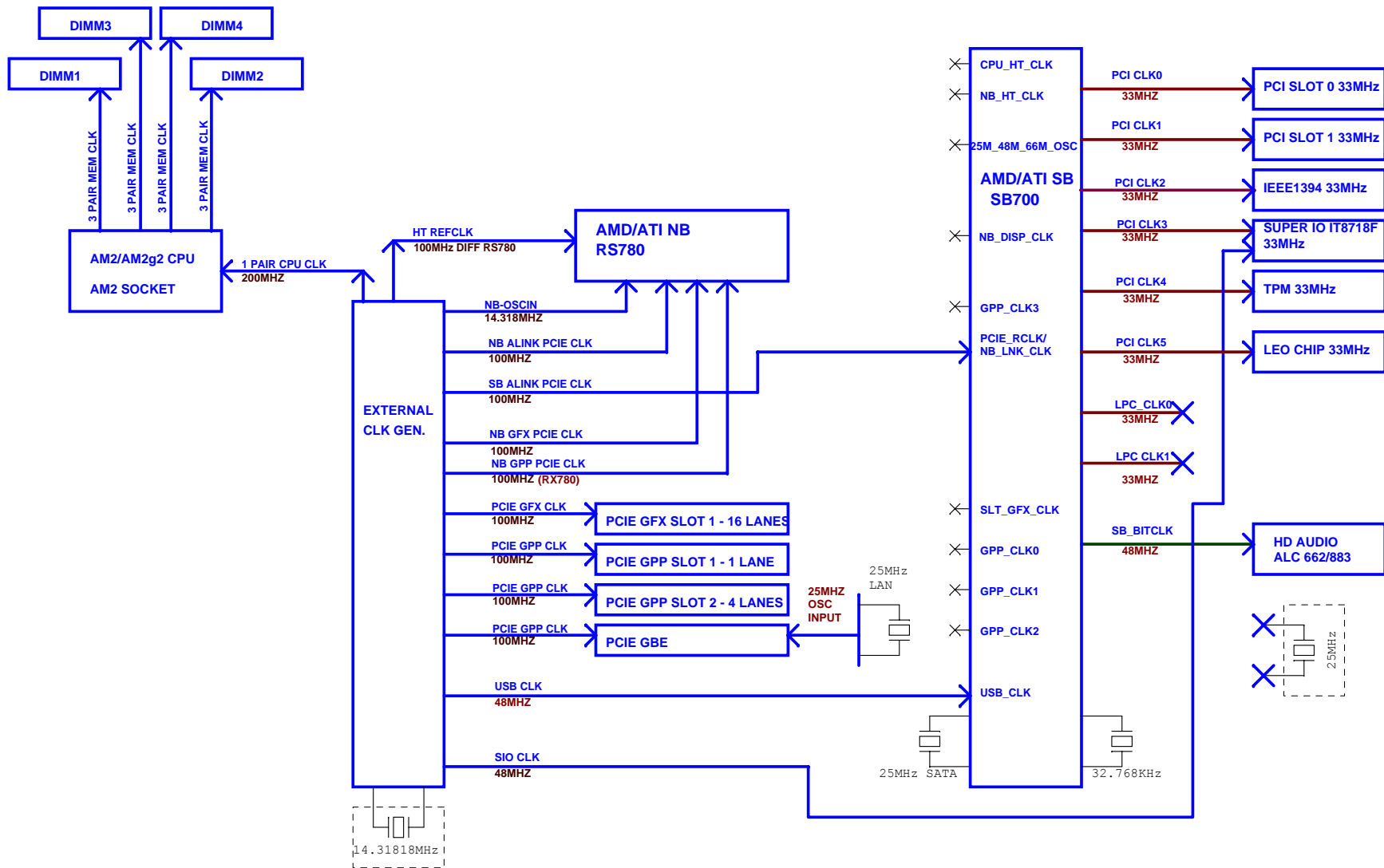
GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

## Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

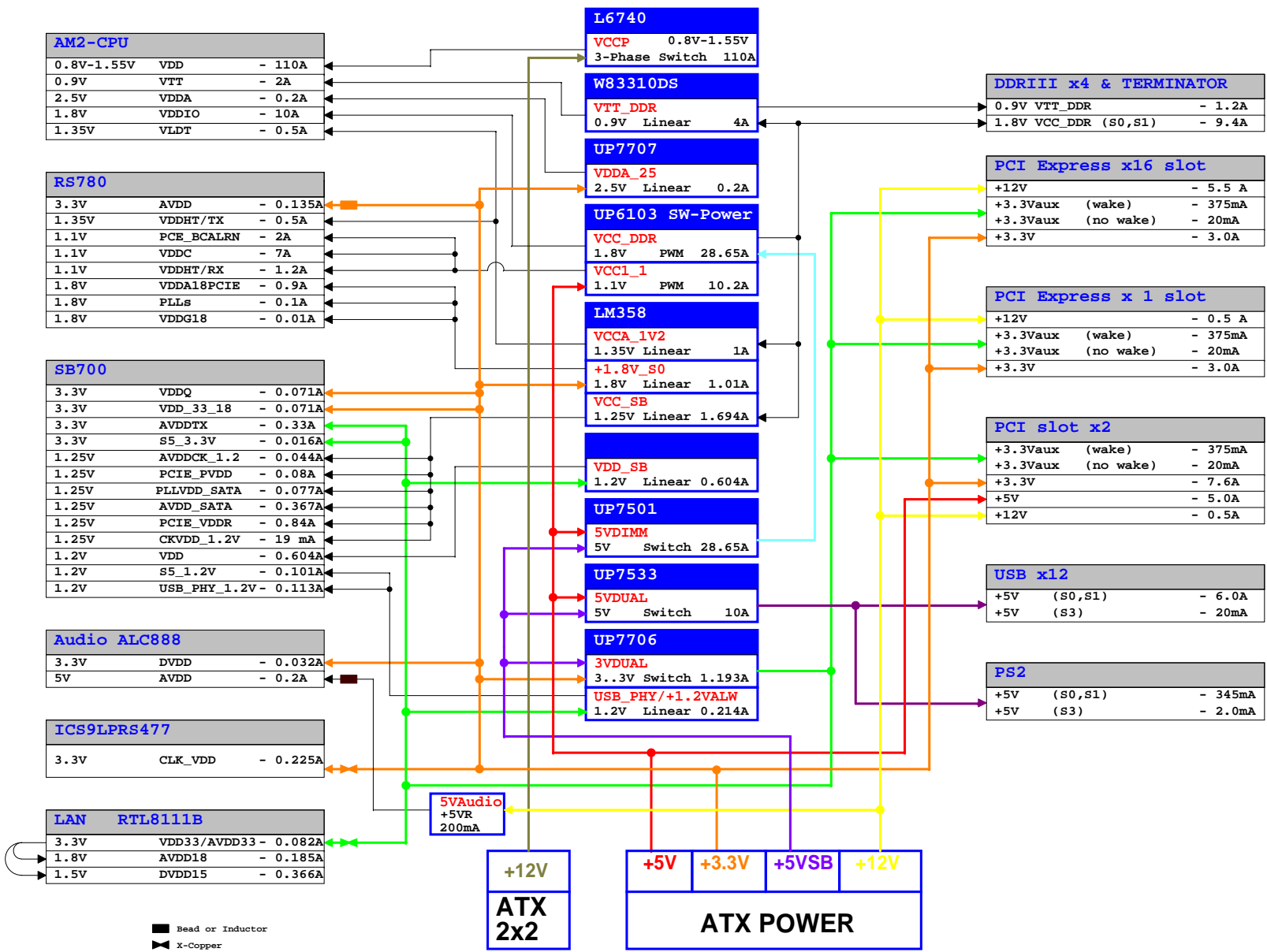
## PCI Config.

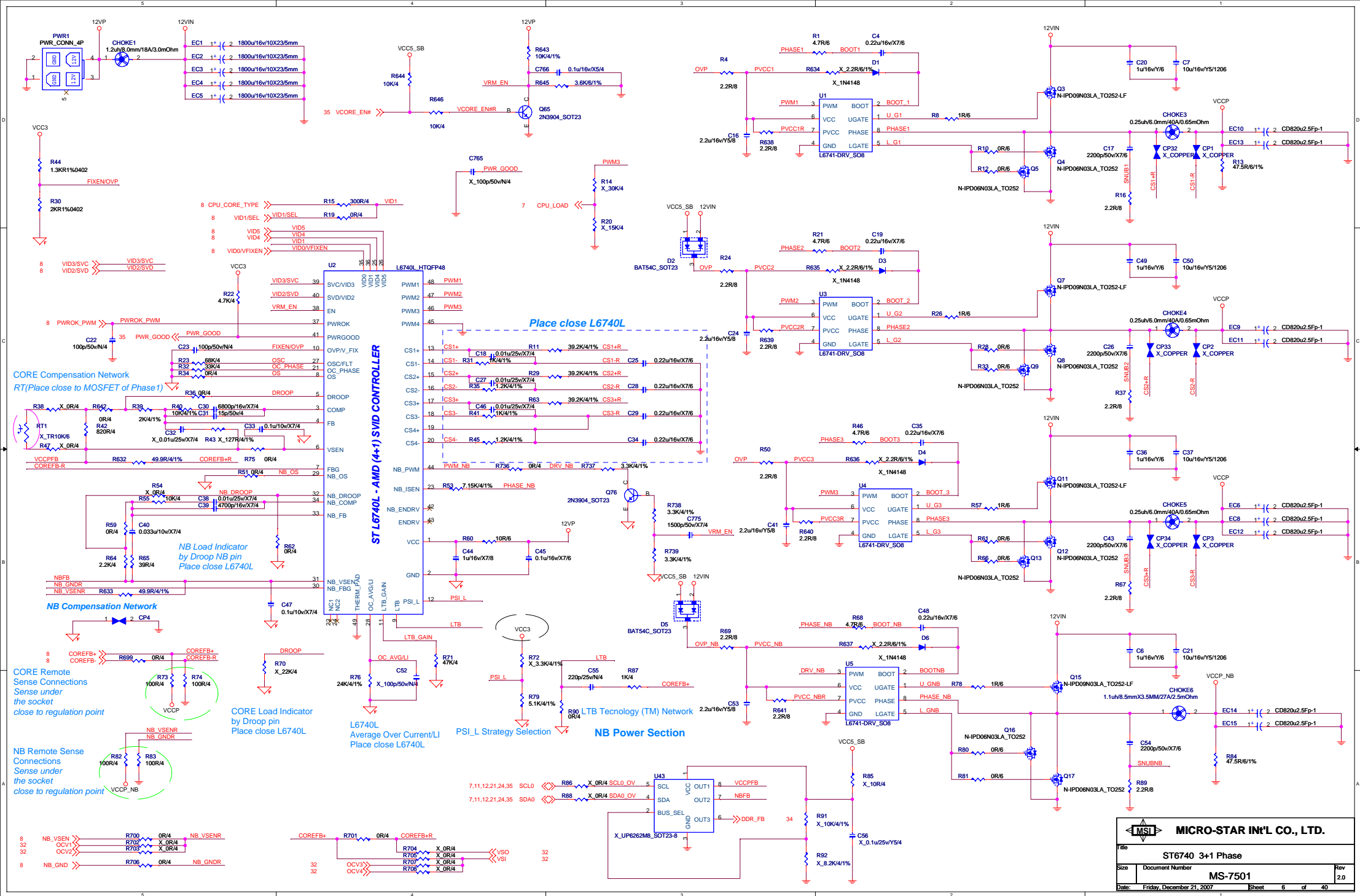
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD18	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD19	PCICLK1
PCI Slot 1	PCI_INTG# PCI_INTH# PCI_INTE# PCI_INTF#	PREQ#2 PGNT#2	AD17	PCICLK2

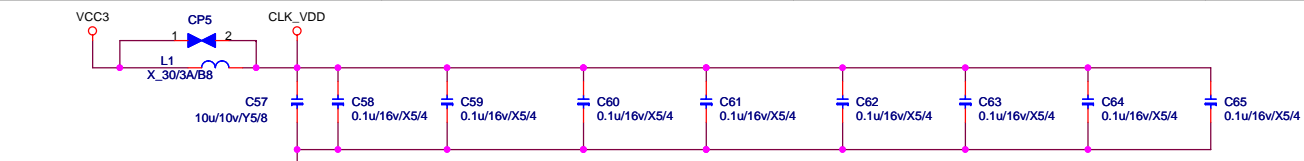


External clock mode  
Internal clock mode

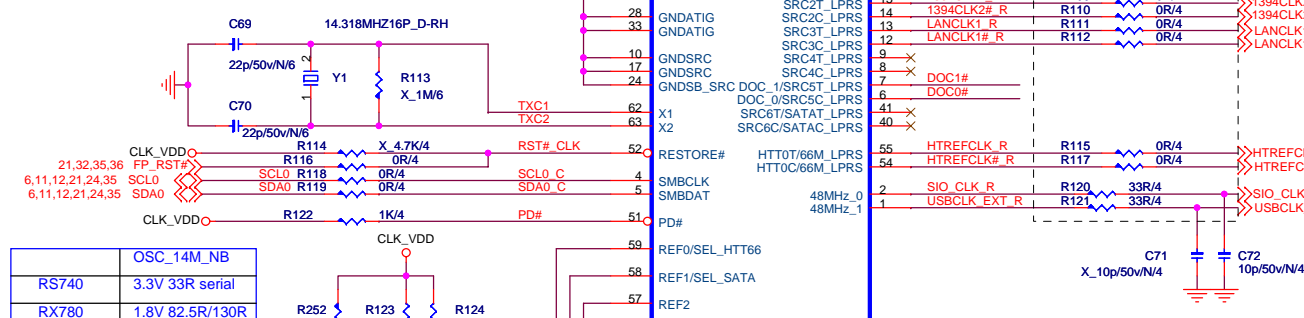
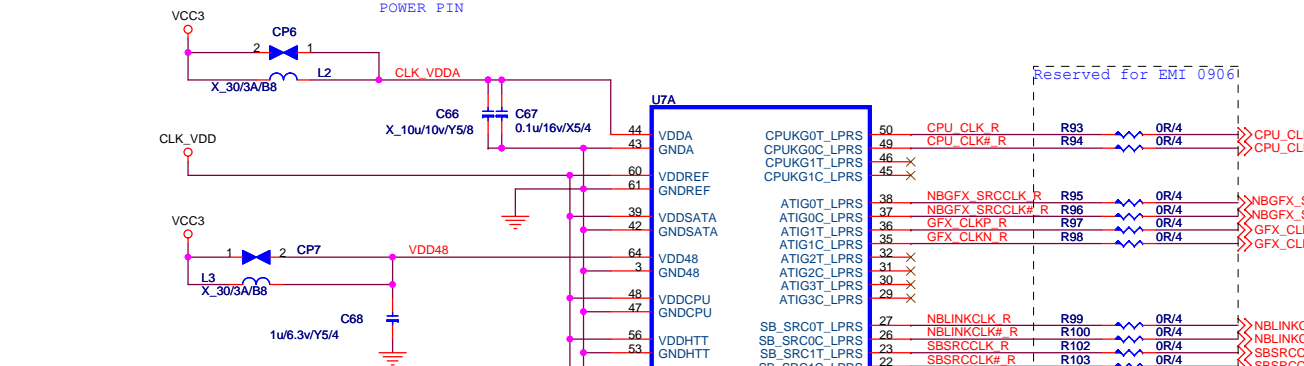
Power Deliver Chart



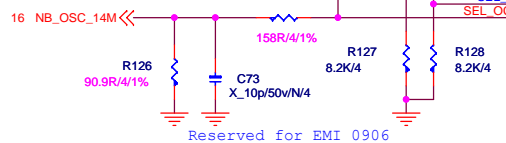




- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U41 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U41 POWER PIN



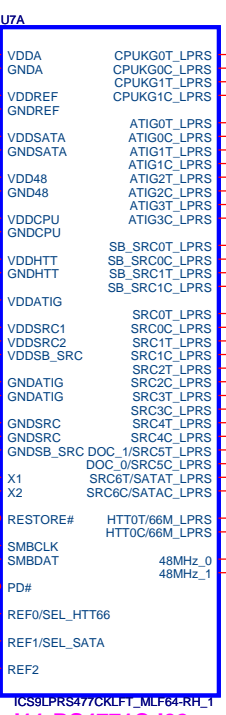
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

### EXT CLK FREQUENCY SELECT TABLE(MHZ)

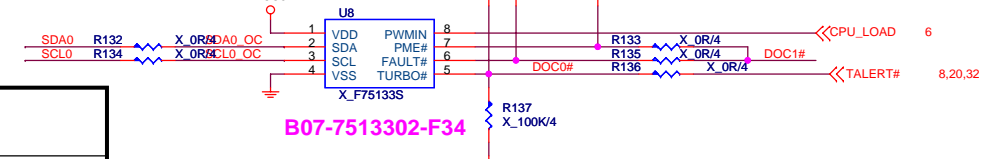
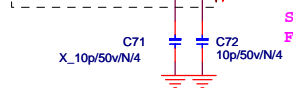
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation



I11-RS4771C-I02

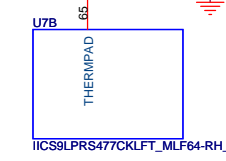
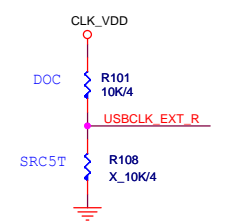
U8, R132, R134, R129, R130, R131, R133, R135, R137 Nc / R136 Stuff  
U8, R132, R134, R129, R131, R133 Stuff / R136, R130, R135, R137 Nc  
R116 if Nc

Reserved for EMI 0906



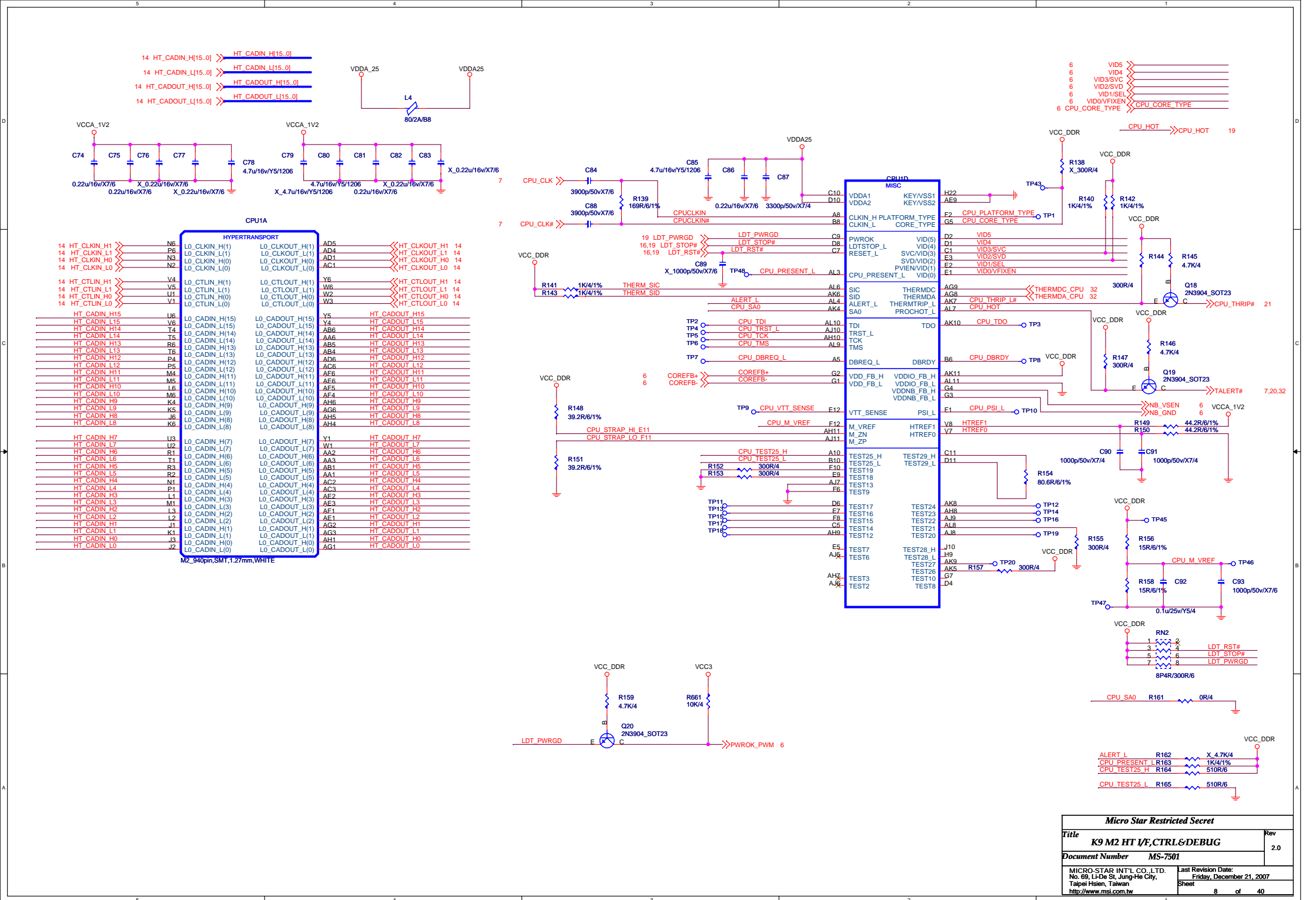
SB700 Pin C8 USBCLK/14M\_25M\_48M\_OSC  
Function set output pin by BIOS.

B07-7513302-F34

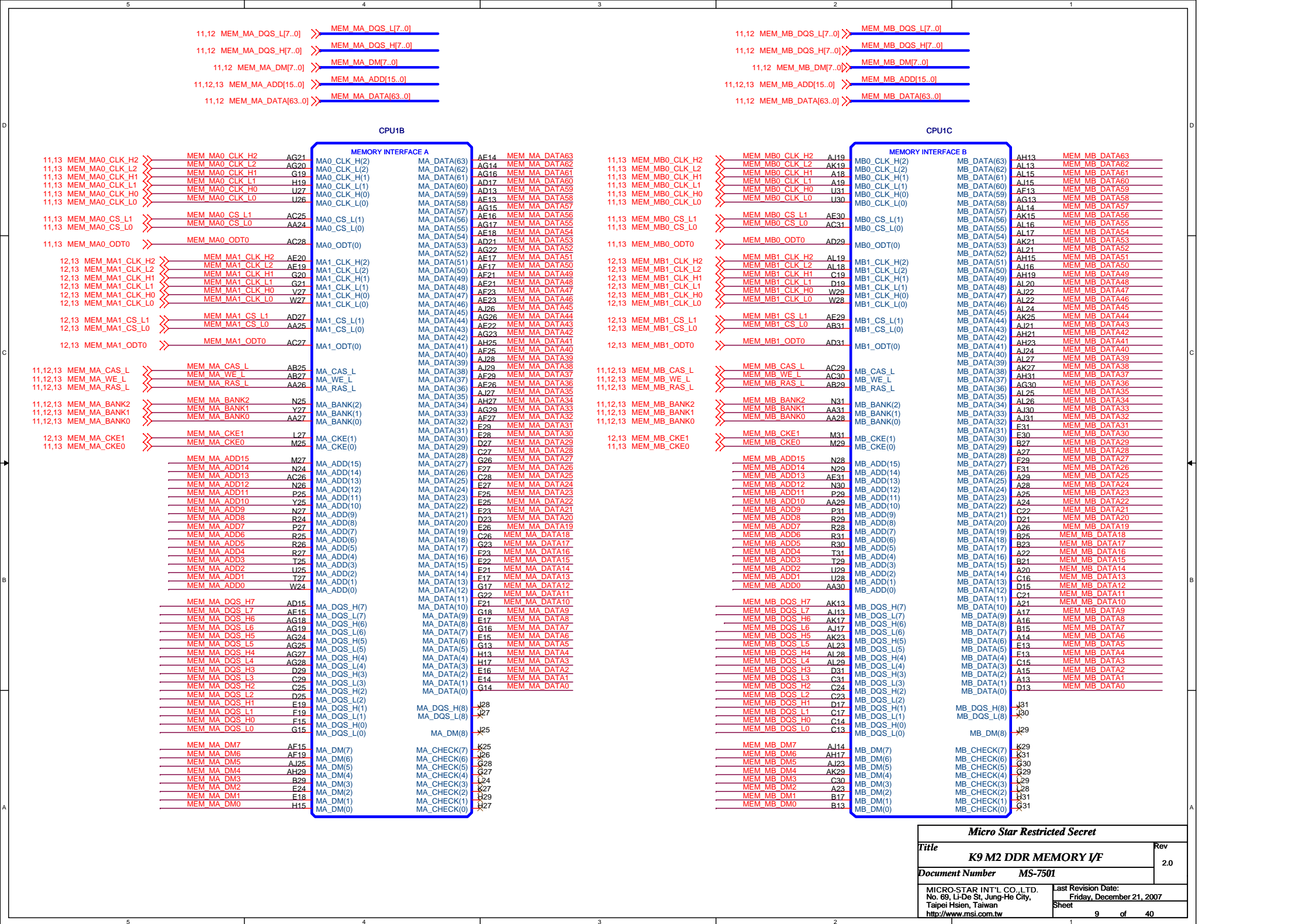


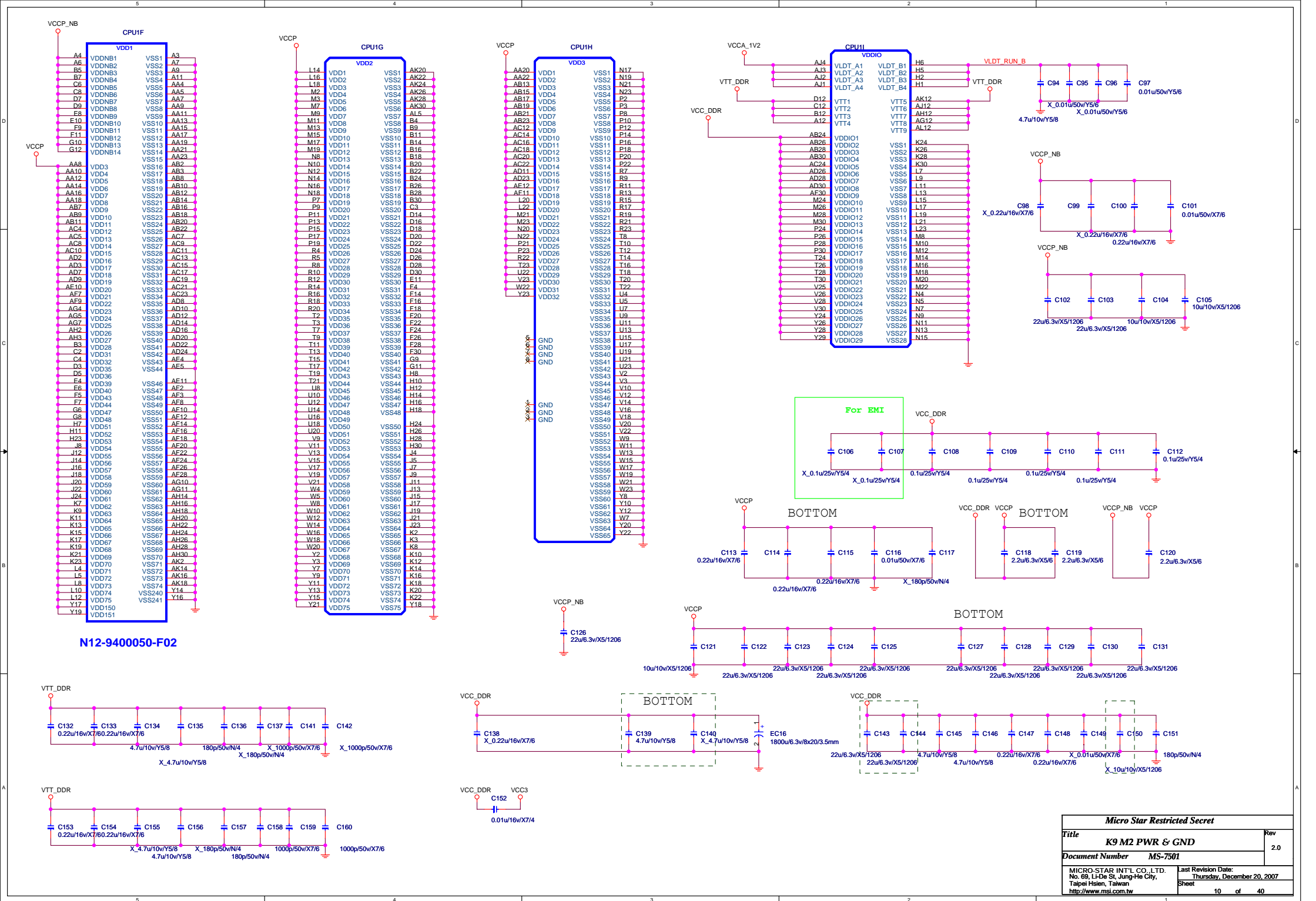
Micro Star Restricted Secret		
Title	Clock-Gen ICS9LPRS477	Rev
Document Number	MS-7501	2.0
MICRO STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, December 21, 2007
Sheet		7 of 40

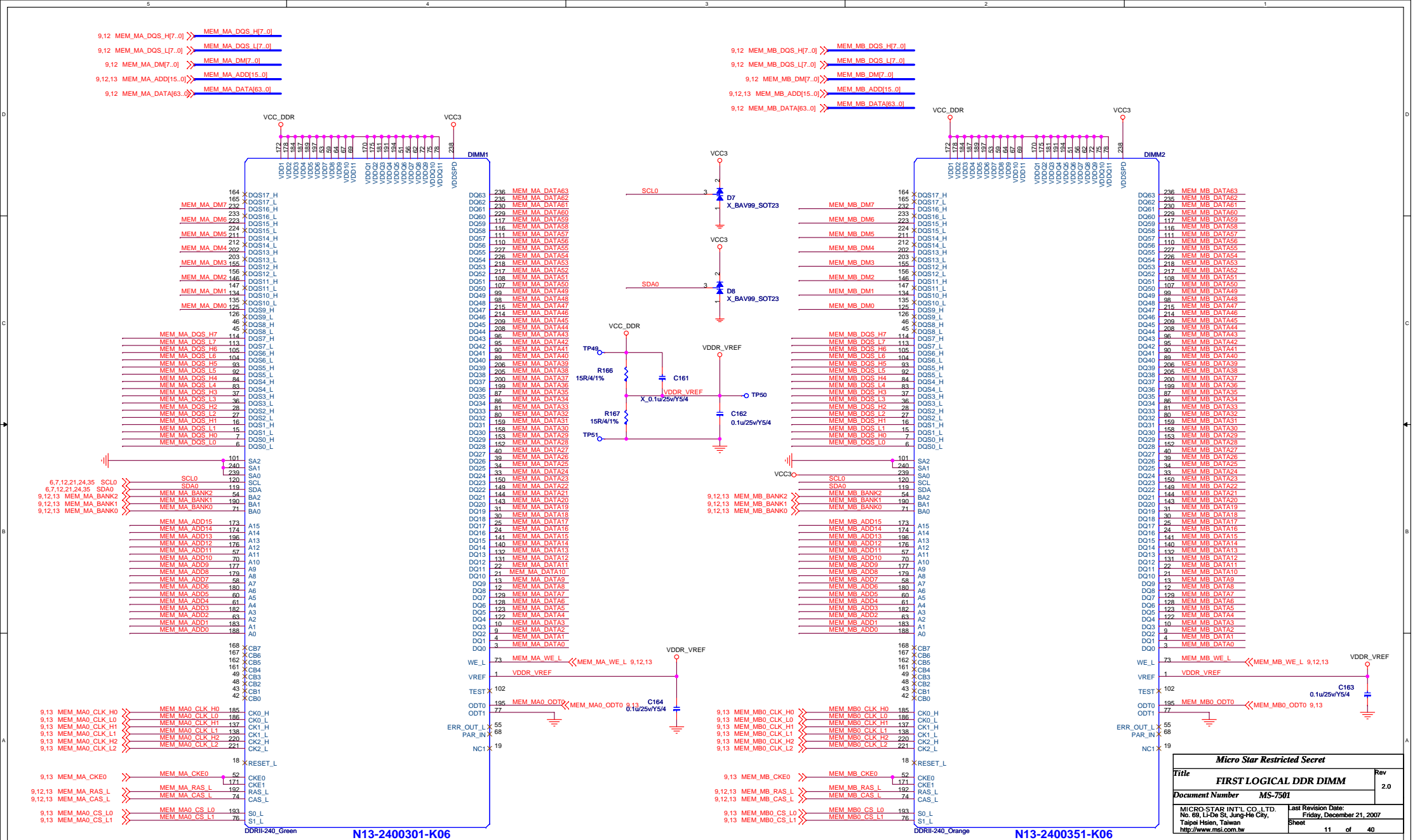








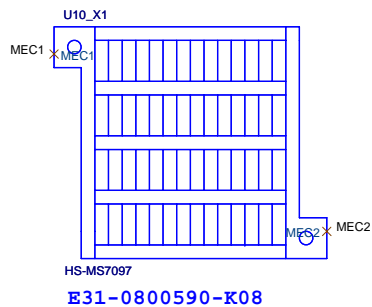








## NB HEAT-SINK



8 HT\_CADOUT\_H[15..0] >> HT\_CADOUT\_H[15..0]  
8 HT\_CADOUT\_L[15..0] >> HT\_CADOUT\_L[15..0]

8 HT\_CADIN\_H[15..0] >> HT\_CADIN\_H[15..0]  
8 HT\_CADIN\_L[15..0] >> HT\_CADIN\_L[15..0]

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20 / 5 / 5 / 5 / 20

U10A  
HT\_CADOUT\_H0 Y25  
HT\_CADOUT\_L0 Y24  
HT\_CADOUT\_H1 V22  
HT\_CADOUT\_L1 V23  
HT\_CADOUT\_H2 V25  
HT\_CADOUT\_L2 V24  
HT\_CADOUT\_H3 U24  
HT\_CADOUT\_L3 U25  
HT\_CADOUT\_H4 T25  
HT\_CADOUT\_L4 T24  
HT\_CADOUT\_H5 P23  
HT\_CADOUT\_L5 P22  
HT\_CADOUT\_H6 P25  
HT\_CADOUT\_L6 P24  
HT\_CADOUT\_H7 N24  
HT\_CADOUT\_L7 N25  
HT\_CADOUT\_H8 AC24  
HT\_CADOUT\_L8 AC25  
HT\_CADOUT\_H9 AB25  
HT\_CADOUT\_L9 AB24  
HT\_CADOUT\_H10 AA24  
HT\_CADOUT\_L10 AA25  
HT\_CADOUT\_H11 Y22  
HT\_CADOUT\_L11 Y23  
HT\_CADOUT\_H12 W21  
HT\_CADOUT\_L12 W20  
HT\_CADOUT\_H13 V21  
HT\_CADOUT\_L13 V20  
HT\_CADOUT\_H14 U20  
HT\_CADOUT\_L14 U21  
HT\_CADOUT\_H15 U19  
HT\_CADOUT\_L15 U18

PART 1 OF 6

HYPER TRANSPORT CPU  
I/F

HT\_TXCAD0P D24  
HT\_TXCAD0N D25  
HT\_TXCAD1P E24  
HT\_TXCAD1N E25  
HT\_TXCAD2P F24  
HT\_TXCAD2N F25  
HT\_TXCAD3P F22  
HT\_TXCAD3N F23  
HT\_TXCAD4P H23  
HT\_TXCAD4N H22  
HT\_TXCAD5P J25  
HT\_TXCAD5N J24  
HT\_TXCAD6P K24  
HT\_TXCAD6N K25  
HT\_TXCAD7P K23  
HT\_TXCAD7N K22  
HT\_TXCAD8P F21  
HT\_TXCAD8N G21  
HT\_TXCAD9P G20  
HT\_TXCAD9N H21  
HT\_TXCAD10P J20  
HT\_TXCAD10N J21  
HT\_TXCAD11P J18  
HT\_TXCAD11N K17  
HT\_TXCAD12P L19  
HT\_TXCAD12N L18  
HT\_TXCAD13P M19  
HT\_TXCAD13N L18  
HT\_TXCAD14P M21  
HT\_TXCAD14N P21  
HT\_TXCAD15P P18  
HT\_TXCAD15N M18

8 HT\_CLKOUT\_H0 >>  
8 HT\_CLKOUT\_L0 >>  
8 HT\_CLKOUT\_H1 >>  
8 HT\_CLKOUT\_L1 >>  
8 HT\_CTLOUT\_H0 >>  
8 HT\_CTLOUT\_L0 >>  
8 HT\_CTLOUT\_H1 >>  
8 HT\_CTLOUT\_L1 >>

T22 HT\_RXCLK0P  
T23 HT\_RXCLK0N  
AB23 HT\_RXCLK1P  
AA22 HT\_RXCLK1N  
M22 HT\_RXCTL0P  
M23 HT\_RXCTL0N  
R21 HT\_RXCTL1P  
R20 HT\_RXCTL1N

301R/4/1% R172 HT\_RXCALP  
HT\_RXCALN A24

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H24 HT\_TXCLK0P  
H25 HT\_TXCLK0N  
L21 HT\_TXCLK1P  
L20 HT\_TXCLK1N  
M24 HT\_TXCTL0P  
M25 HT\_TXCTL0N  
P19 HT\_TXCTL1P  
R18 HT\_TXCTL1N

8 HT\_CLKIN\_H0 >>  
8 HT\_CLKIN\_L0 >>  
8 HT\_CLKIN\_H1 >>  
8 HT\_CLKIN\_L1 >>  
8 HT\_CTLIN\_H0 >>  
8 HT\_CTLIN\_L0 >>  
8 HT\_CTLIN\_H1 >>  
8 HT\_CTLIN\_L1 >>

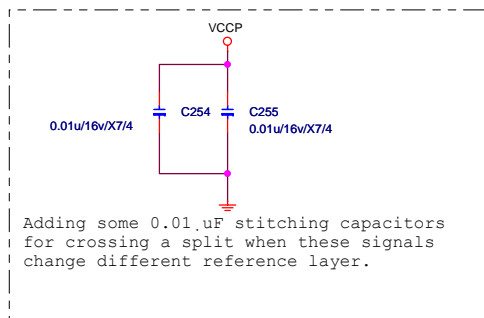
B24 HT\_TXCALP  
B25 HT\_TXCALN

5 / 10

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

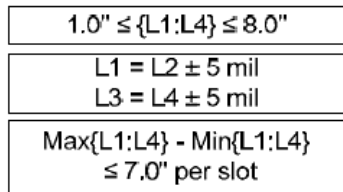
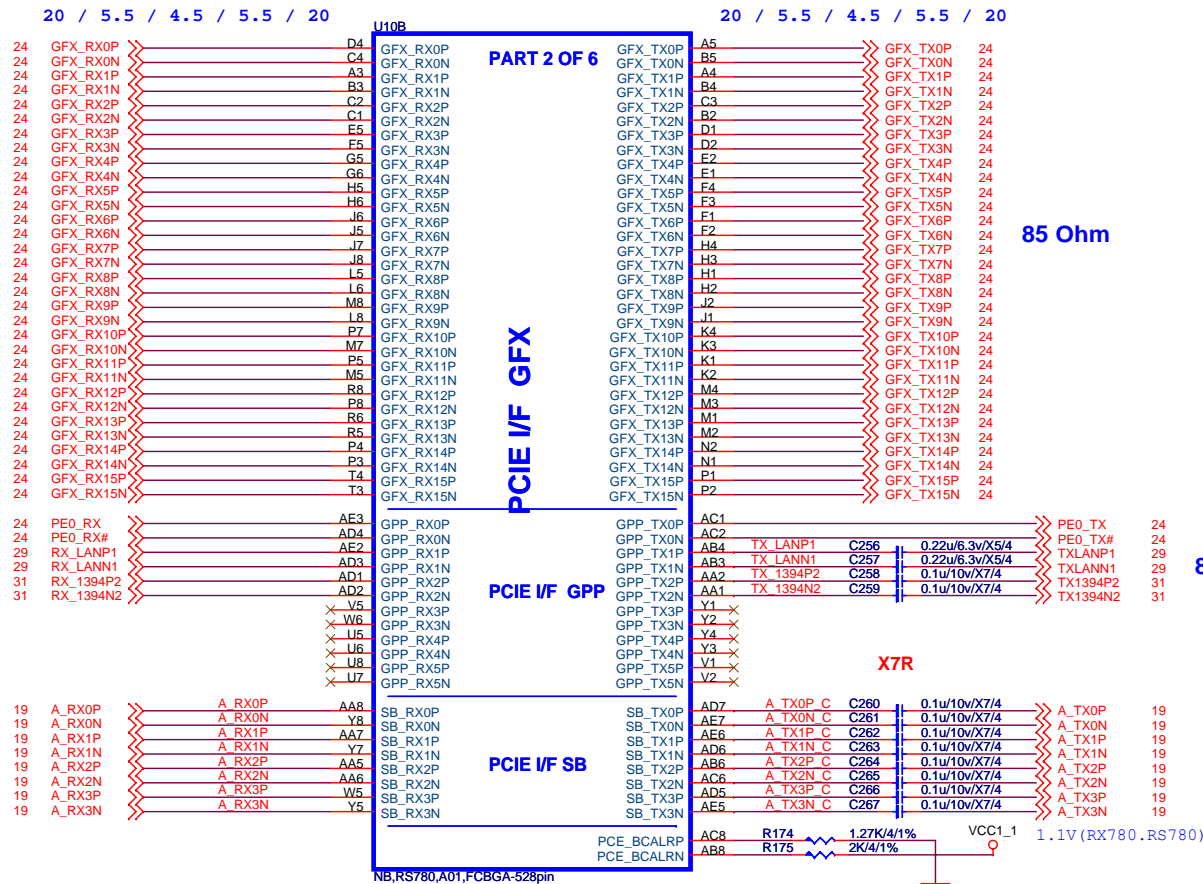
SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



MICRO-STAR IN'L CO., LTD.

Title			RS780-HT L
Size	Document Number	MS-7501	
Date:	Friday, December 21, 2007	Sheet	14 of 40
			Rev 2.0





RS780

GPP\_RXnP

GPP\_RXnN

GPP\_TXnP

GPP\_TXnN

PCI-E Expansion  
Connector or  
Device

PERp(x)

PERn(x)

PETp(y)

PETn(y)

RS780 Display Port Support (muxed on GFX)

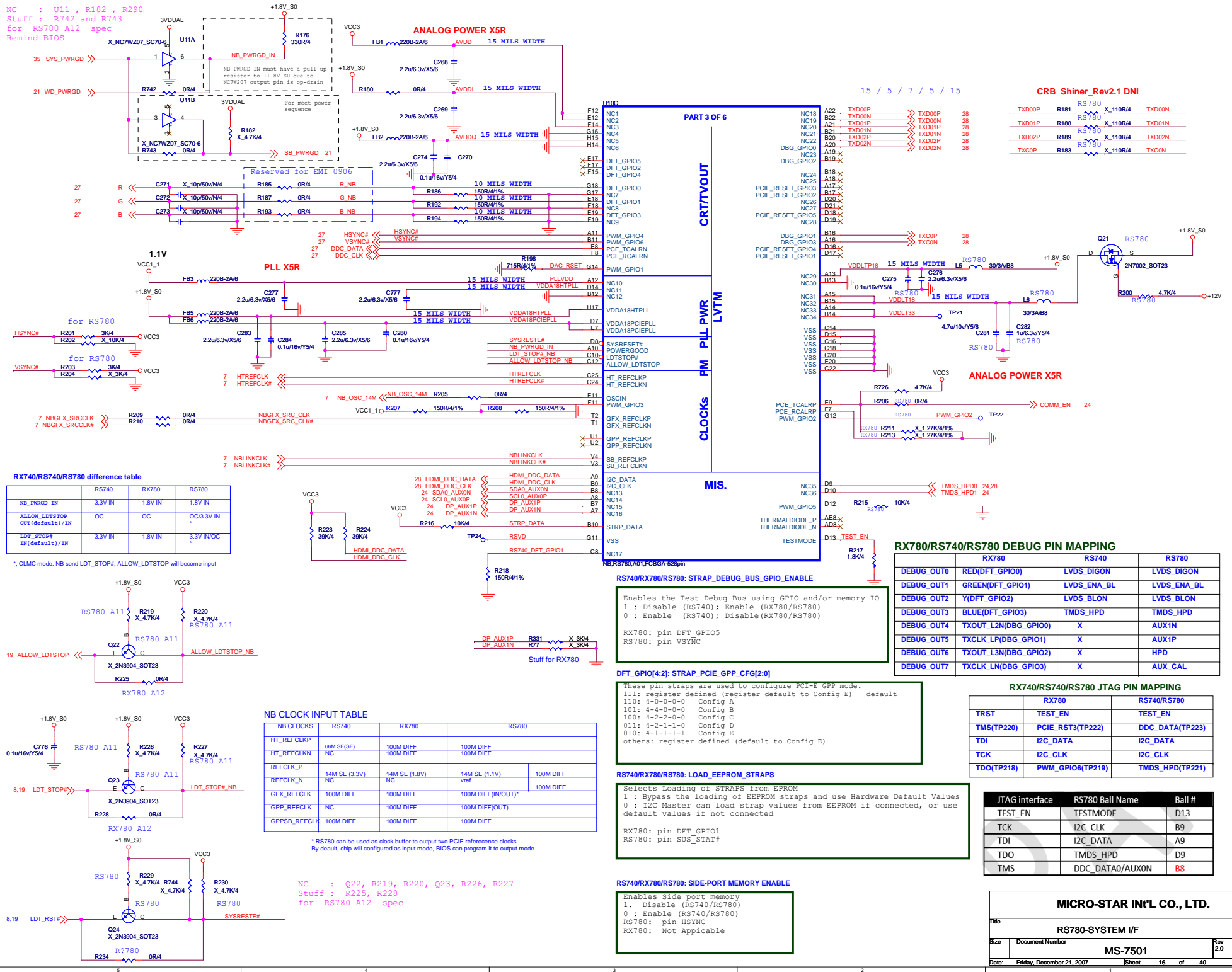
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

MICRO-STAR INT'L CO., LTD.			
Title RS780-PCIE I/F			
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NC : U11, R182, R290  
Stuff : R742 and R743  
for RS780 A12 spec  
Remind BIOS



**RX740/RS740/RS780 difference table**

	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP_OUT(default)/IN	OC	OC	OC/3.3V IN
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC

\* CLMC mode: NB send LDT\_STOP#, ALLOW\_LDTSTOP will become input

**RX780/RS740/RS780 DEBUG PIN MAPPING**

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMD5_HPD	TMD5_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

**RX740/RS740/RS780 JTAG PIN MAPPING**

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMD5_HPD(TP221)

**JTAG interface**

RS780 Ball Name	Ball #
TEST_EN	D13
TCK	B9
TDI	A9
TDO	D9
TMS	DDC_DATA/AUXON

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**RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE**

Enables the Test Debug Bus using GPIO and/or memory IO  
1 : Disable (RS740); Enable (RX780/RS780)  
0 : Enable (RS740); Disable (RX780/RS780)

RX780: pin DFT\_GPIO5  
RS780: pin VSYNC

**DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]**

These pin straps are used to configure PCI-E GPP mode.  
110: register defined (register default to Config E) default  
110: 4-0-0-0-0 Config A  
101: 4-4-0-0-0 Config B  
100: 4-2-2-0-0 Config C  
011: 4-2-1-1-0 Config D  
010: 4-1-1-1-1 Config E  
others: register defined (default to Config E)

**RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

RX780: pin DFT\_GPIO1  
RS780: pin SUS\_STAT#

**RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE**

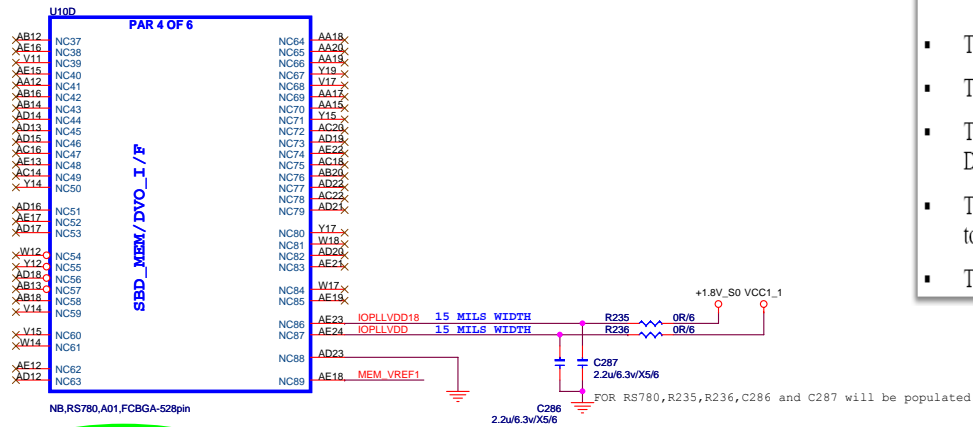
Enables Side port memory  
1. Disable (RS740/RS780)  
0 : Enable (RS740/RS780)  
RS780: pin HSYNC  
RX780: Not Applicable

**NB CLOCK INPUT TABLE**

	RS740	RX780	RS780
HT_REFCLKP	60M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

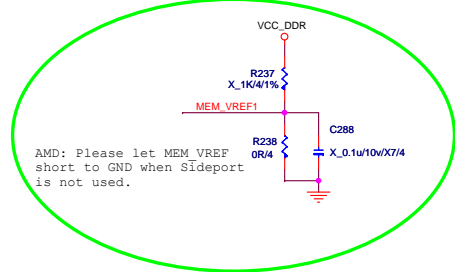
\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

NC : Q22, R219, R220, Q23, R226, R227  
Stuff : R225, R228  
for RS780 A12 spec



Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD\_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18\_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM\_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD018 is connected to 1.8 V and IOPLLVD0 is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT\_GPIO0 is **not** connected to the GND.



## Max Power Estimates for RS780 and SB700

(Preliminary Data w/ Internal Clock Generator and IMC disabled)

April 2007

Voltage	Usage	Domain	Max(Spec)
1.0-1.1V	RS780	S0/S1	10A
1.1V	RS780	S0/S1	3-4A
1.2V	RS780 & SB700	S0/S1	2.4A (1A-NB / 1.4A-SB)
1.8V	RS780& SB700	S0/S1	0.8A (0.75A-NB / 50mA-SB)

## Max Power Estimates for RS780 and SB700 (continued)

April 2007

Voltage	Usage	Domain	Max(Spec)
3.3V	RS780& SB700	S0/S1	428mA (0.3A-NB / 128mA-SB)
1.2VDual	SB700	S0/S1/S2/S3/S4/S5	217mA
3.3VDual	SB700	S0/S1/S2/S3/S4/S5	495mA
5V	SB700 V5_VREF	S0/S1	0.21mA

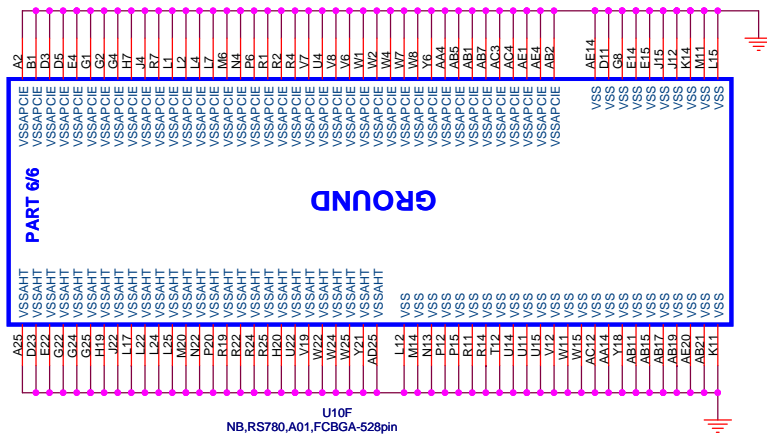
MICRO-STAR INT'L CO., LTD.

File RS780-SPMEM/STRAPS

Size Document Number MS-7501

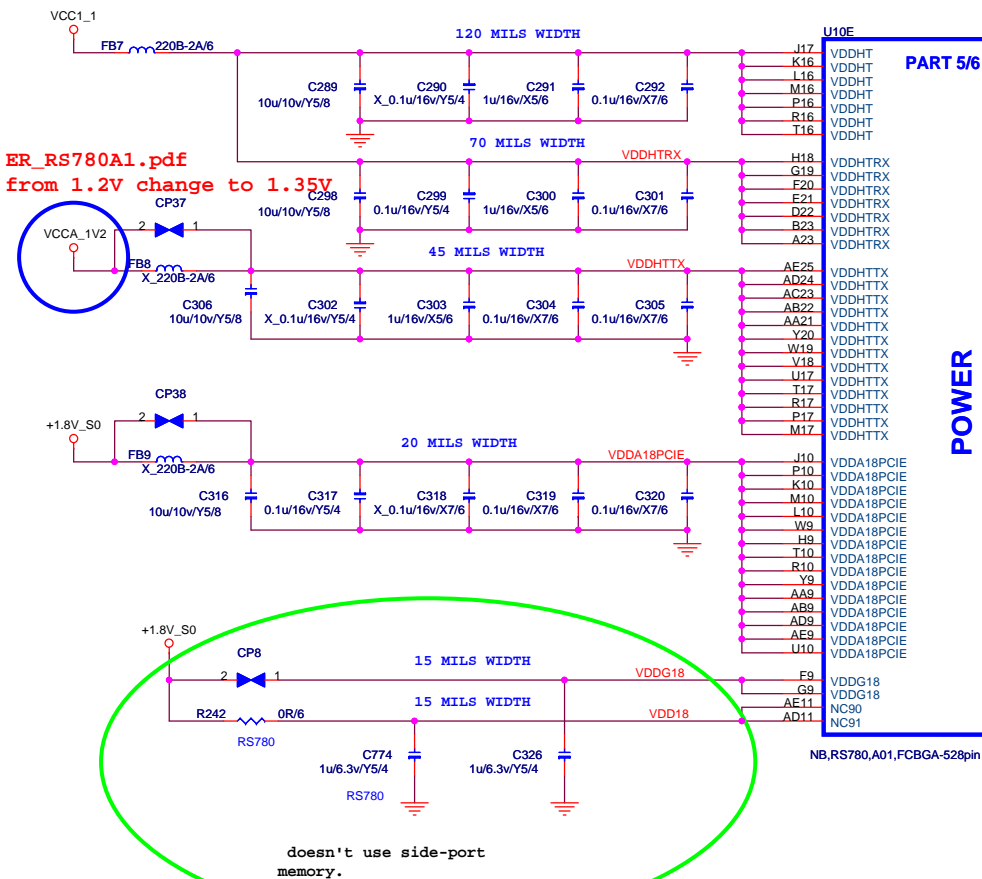
Date: Thursday, December 20, 2007 Sheet 17 of 40

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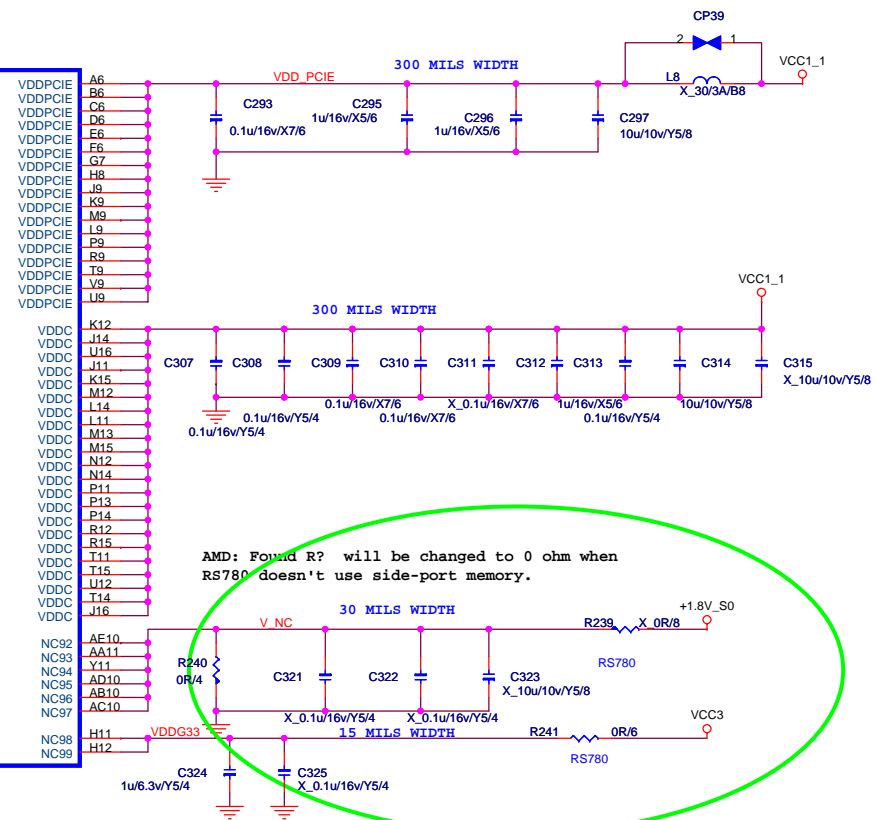


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



POWER



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## U13\_X1

MSI

SB\_HEATSINK  
7388

PLACE PCIE

100 Ohm

100 Ohm

PLACE THESE COMPONENTS CLOSE TO U600, AND  
USE GROUND GUARD FOR 32K X1 AND 32K X2

Note: LDT\_PG, LDT\_STP# & LDT\_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

### Check U13 New Version : Port Number

```

| SIO PCICLK has been chaneged
| PCICLK5 to PCICLK4 for AMD
| recommand

```

For EMI

10 pf For SA

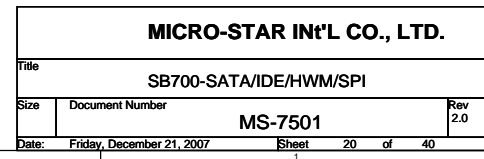
Adding some 0.1.uF stitching capacitors for crossing a split when these signals change different reference layer.

**MICRO-STAR INT'L CO., LTD.**

Title	SB700-PCIE/PCI/CPU/LPC
-------	------------------------

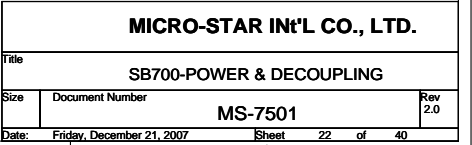
Size	Document Number
	MS-7501

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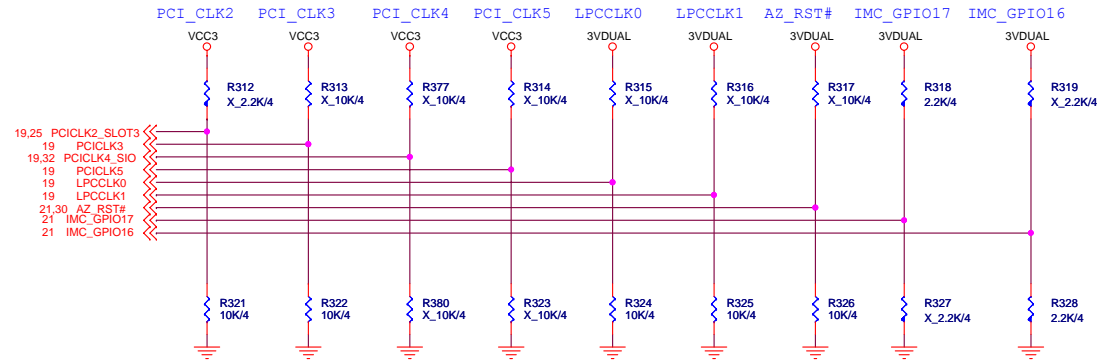






## REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM DEFAULT	

## DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

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# PCI Express Slot x16/x1

6,7,11,12,21,35 SCL0  
6,7,11,12,21,35 SDA0

21,29 PE\_WAKE#

30 SPDIF\_PCIE

15 GFX\_TX0P  
15 GFX\_TX0N

16 SCL0\_AUX0P

15 GFX\_TX1P  
15 GFX\_TX1N

15 GFX\_TX2P  
15 GFX\_TX2N

15 GFX\_TX3P  
15 GFX\_TX3N

16 SDA0\_AUX0N

15 GFX\_TX4P  
15 GFX\_TX4N

15 GFX\_TX5P  
15 GFX\_TX5N

15 GFX\_TX6P  
15 GFX\_TX6N

15 GFX\_TX7P  
15 GFX\_TX7N

16,28 TMD5\_HP0D

15 GFX\_TX8P  
15 GFX\_TX8N

15 GFX\_TX9P  
15 GFX\_TX9N

15 GFX\_TX10P  
15 GFX\_TX10N

15 GFX\_TX11P  
15 GFX\_TX11N

15 GFX\_TX12P  
15 GFX\_TX12N

15 GFX\_TX13P  
15 GFX\_TX13N

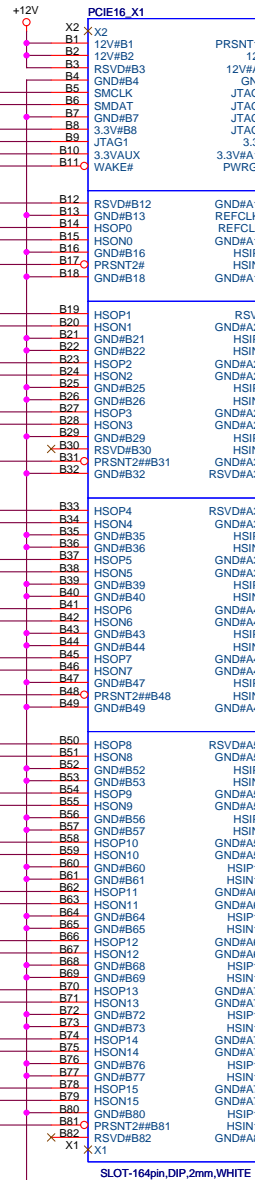
15 GFX\_TX14P  
15 GFX\_TX14N

15 GFX\_TX15P  
15 GFX\_TX15N

TMD5\_HP0D R334

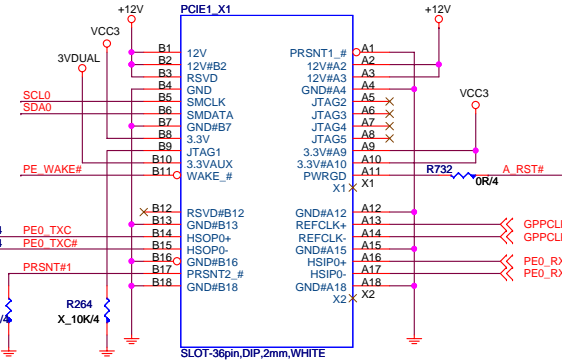
X\_0R/4 PRSNT#2 81

## PCI EXPRESS x16 Slot

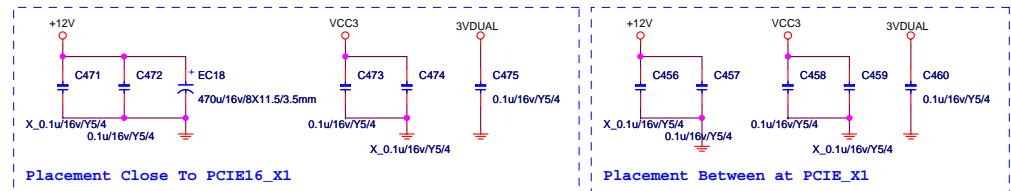


N11-1640401-K06

## PCI EXPRESS 1 Slot-1

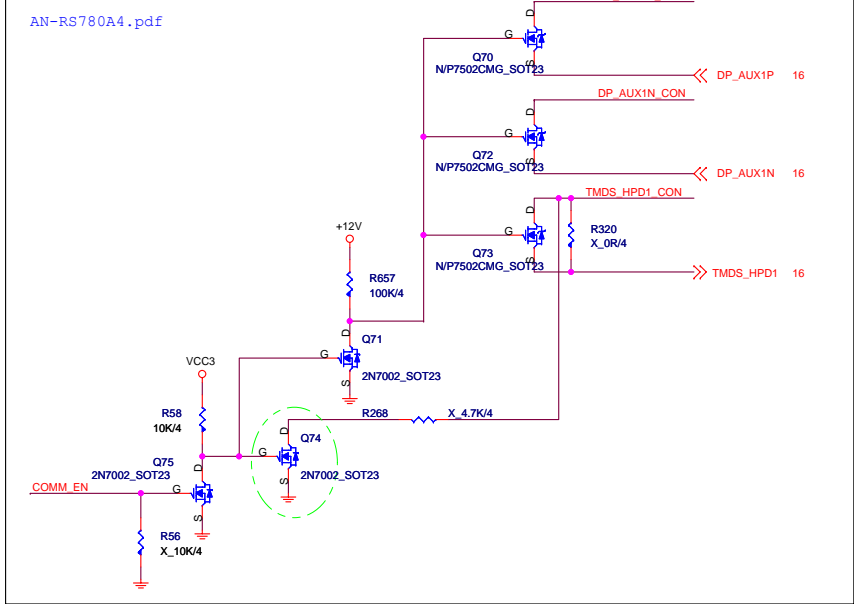


N11-0360091-F02



## Switch circuit for secondary displayport

AN-RS780A4.pdf

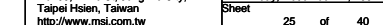


MSI  
Link to the Future  
MICRO-START INT'L CO.,LTD.

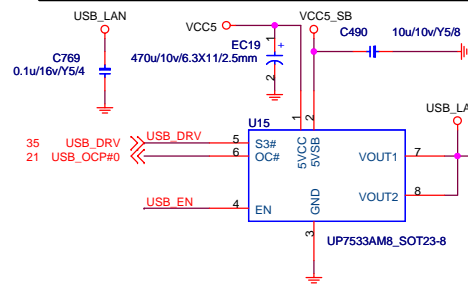
PCI EXPRESS X16 & X1 SLOT

Size Custom Document Number MS-7501 Rev 2.0

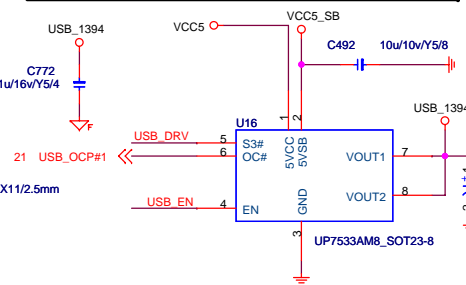
Date: Friday, December 21, 2007 Sheet 24 of 40



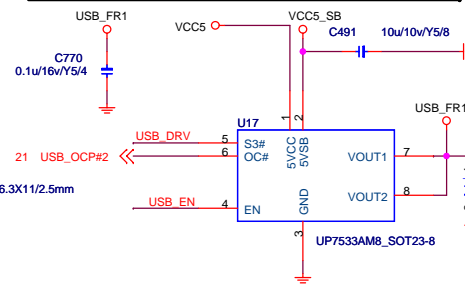
## POWER CIRCUIT FOR USB PORT 4,5



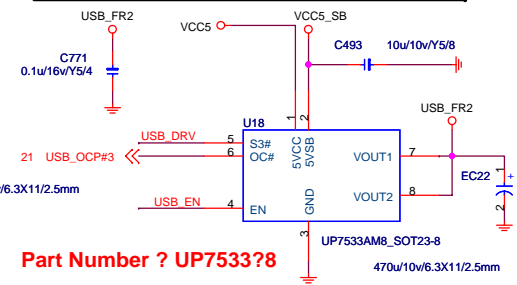
## POWER CIRCUIT FOR USB PORT 2,3



## POWER CIRCUIT FOR USB PORT 0,1



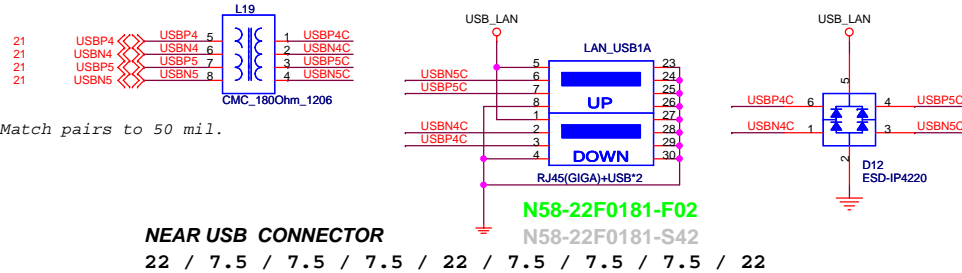
## POWER CIRCUIT FOR USB PORT 6,7



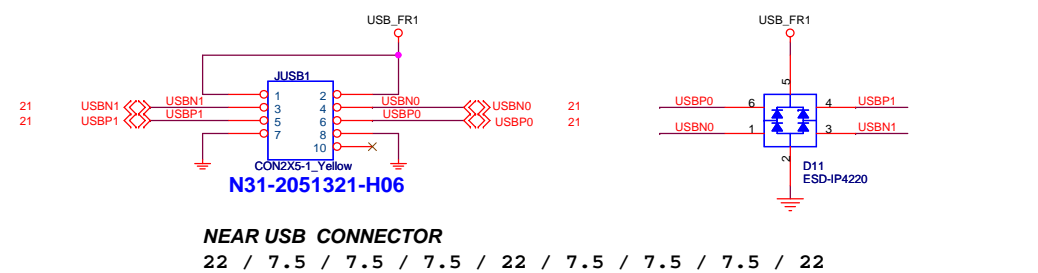
Part Number ? UP7533?8

## REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches

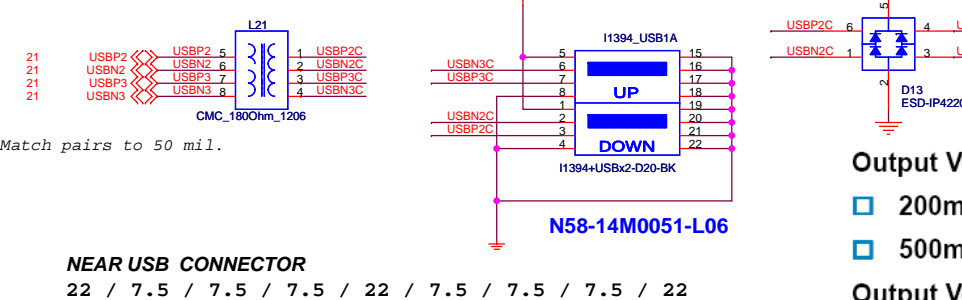


## FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

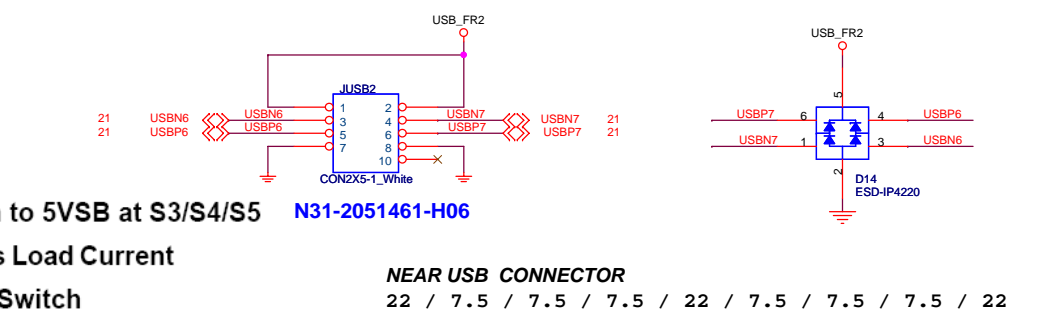


## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



Output Voltage Switch to 5VSB at S3/S4/S5 N31-2051461-H06

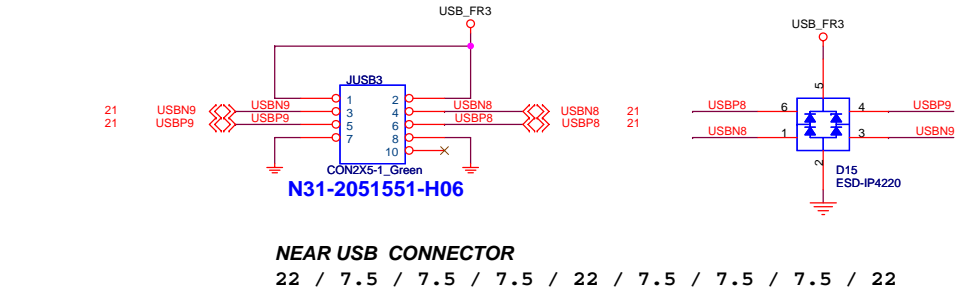
- 200mA Continuous Load Current
- 500mΩ High Side Switch

Output Voltage Switch to 5VCC at S0/S1/S2

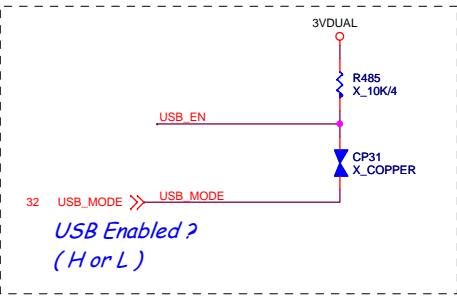
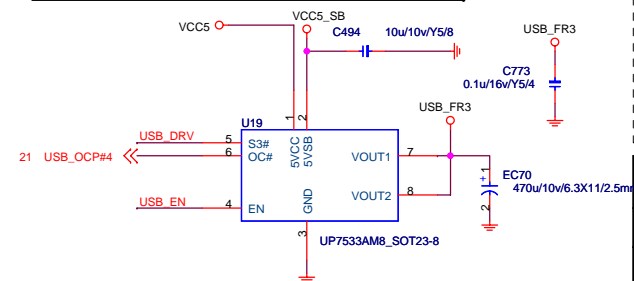
- 1.5A Continuous Load Current
- 110mΩ High Side Switch

## FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



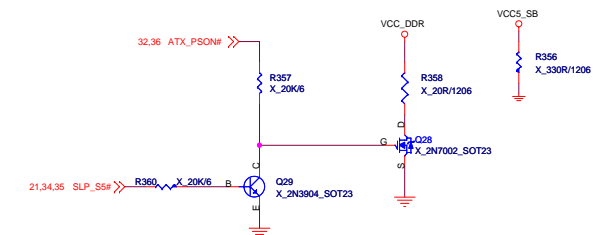
## POWER CIRCUIT FOR USB PORT 8,9



USB Enabled ?  
(H or L)

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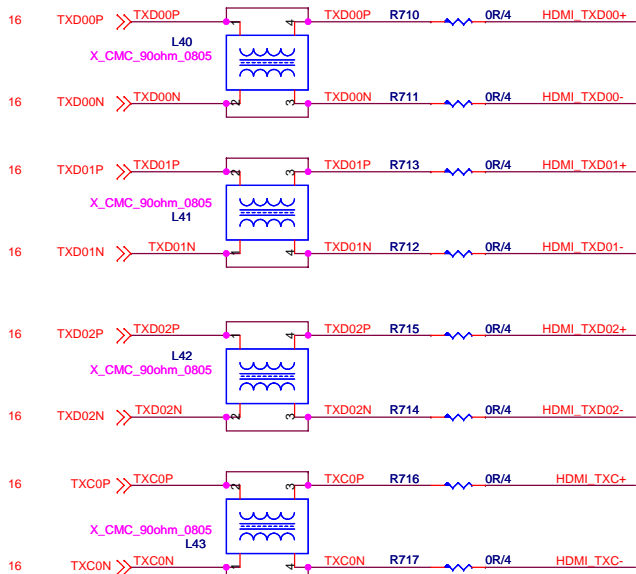
Title			USB Conn.
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[illegible]

T:2 , H:4.5 ,W:5 ,S:7,Er:4.2 ,Zo=104.8 Ohm

CRB Shiner\_Rev2.1 change to 0 Ohm

15 / 5 / 7 / 5 / 15



EMI request 20070910

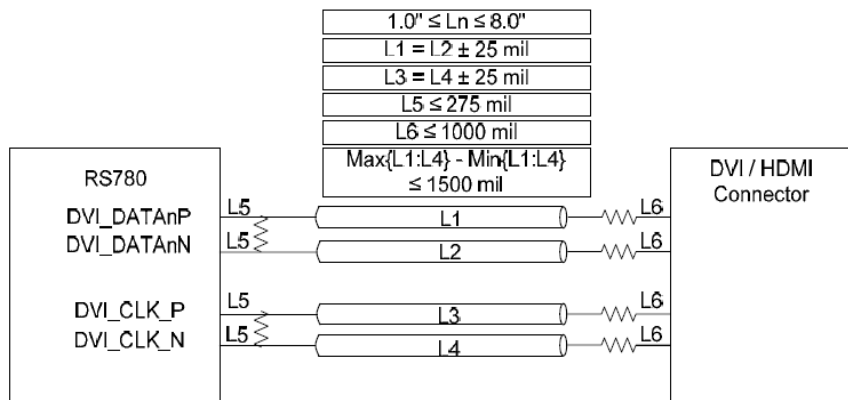
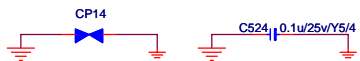
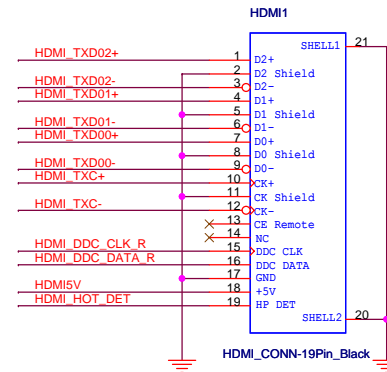
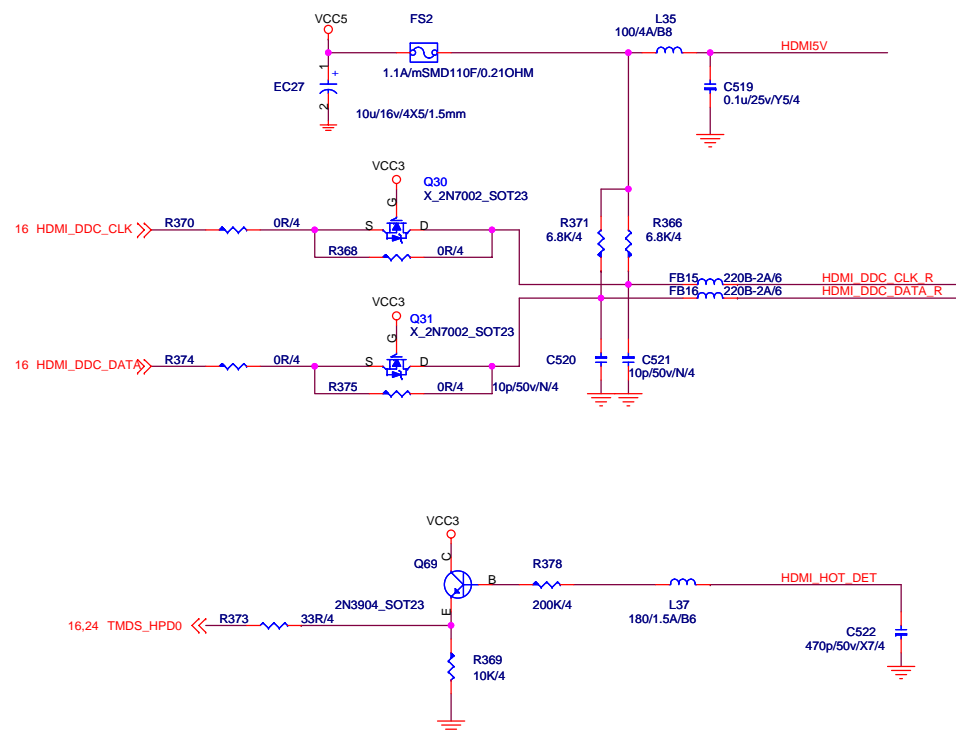


Figure 32: Layout Guidelines for the DVI/HDMI Signals

## HDMI CONNECTOR

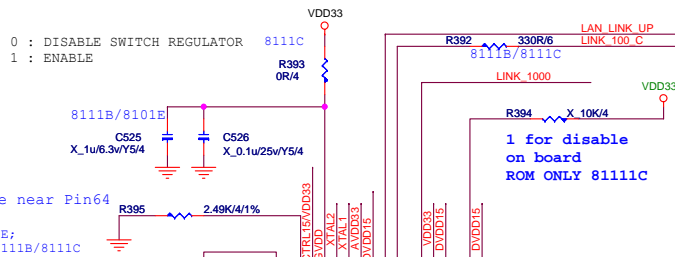


N5I-19M0161-L06

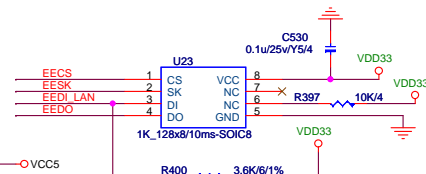


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1. Pin 64:RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.
2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
3. RTL8111B/C/8101E, Pin 1~16 forward to transformer, this will made the trace more short.
4. As the Layout Guide, the output pin of Transistor trace please layout it more widely.
5. Make nine through holes at the center of IC board. The back side of IC is GND. Please be aware to connect this GND to the GND of outside of LAN chip.
6. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
7. The Spec of transistor suggest use the current least 1.2A.
8. 1.5V請留 power plane並且盡量大一點.
9. 1.5V Bypass 電容不能省. Add 0.1u cap. for each power pin of LAN.
10. For RTL8111B, Pin62 有外接兩顆電容絕對不能省.



CHOK7 close to U22 Pin 1 within 0.5cm

VL1.8 CP18 X COPPER EVDD18 C531 0.1u/25w/Y5/4

CTRL18 8111C CHOK7 CH4.7uH1.24A C532 0.1u/25w/Y5/4

VL1.8 CP19 X COPPER AVDD18 C533 22u/6.3w/X5/1206 C534 X 0.1u/25w/Y5/4

C532, C533 CLOSE TO CHOK7

CTRL15 R402 X OR/8 CTRL15/VDD33 R403 X OR/4 DVDD15 CLKREQB R404 X OR/4 AVDD18 FB12

8111B/8101E

8111C VDD33 FB12 R405 OR/4 AVDD18 FB12 R406 OR/8 CTRL15/VDD33

VL1.8 R408 OR/8 DVDD15 C560 22u/6.3w/X5/1206 C561 0.1u/25w/Y5/4

C560, C561 close to U22 Pin 63 within 0.5cm

Power consumption

Giga-Lan

10/100-Lan

Micro Star Restricted Secret

Title LAN - Realtek 8111C(B)/8101E

Document Number MS-7501

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Last Revision Date: Friday, December 21, 2007

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## Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A

For RTL8101E stuff R410, C563 NC

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF

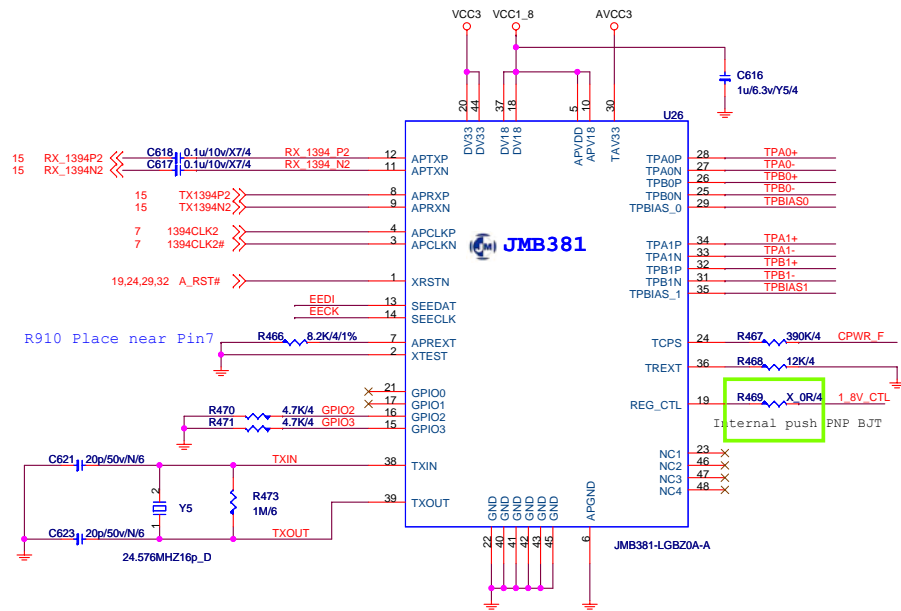
8111B/8111C to 0 ohm 8101E to 0.01uF

8111B/8111C to 0 ohm 8101E to 0.01uF



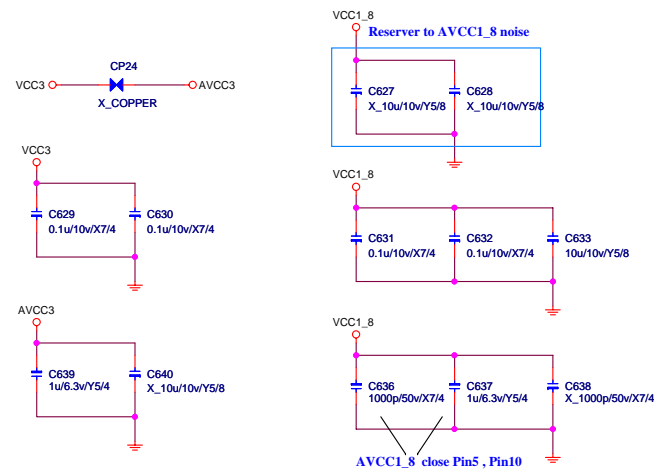


## 1394 CONTROLLER

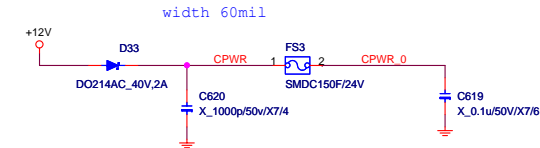
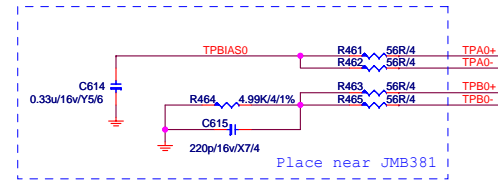


### Table 5.1 JMB381 Operating Modes

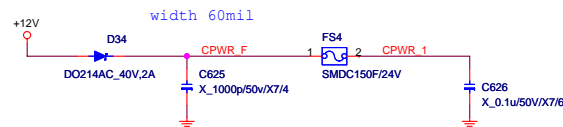
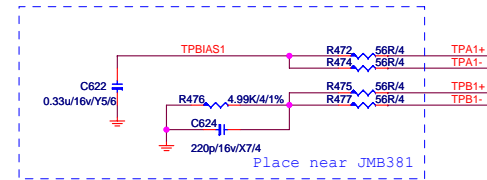
	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1



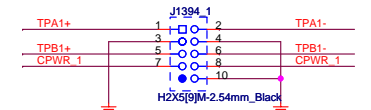
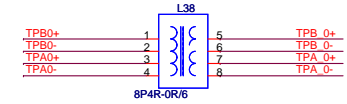
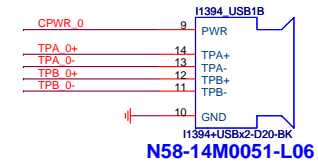
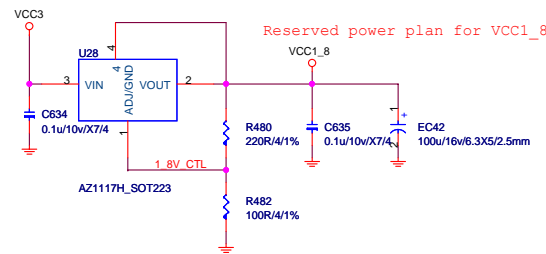
Rear 1394 port



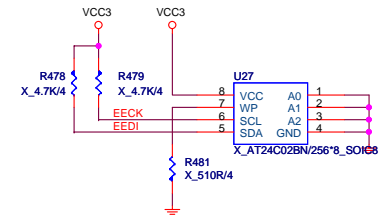
Front 1394 pin header



**A1117 CO-LAY SOT223 (TO\_261) PNP BJT**



For Intel 1394 pinheader



S3 Resume time

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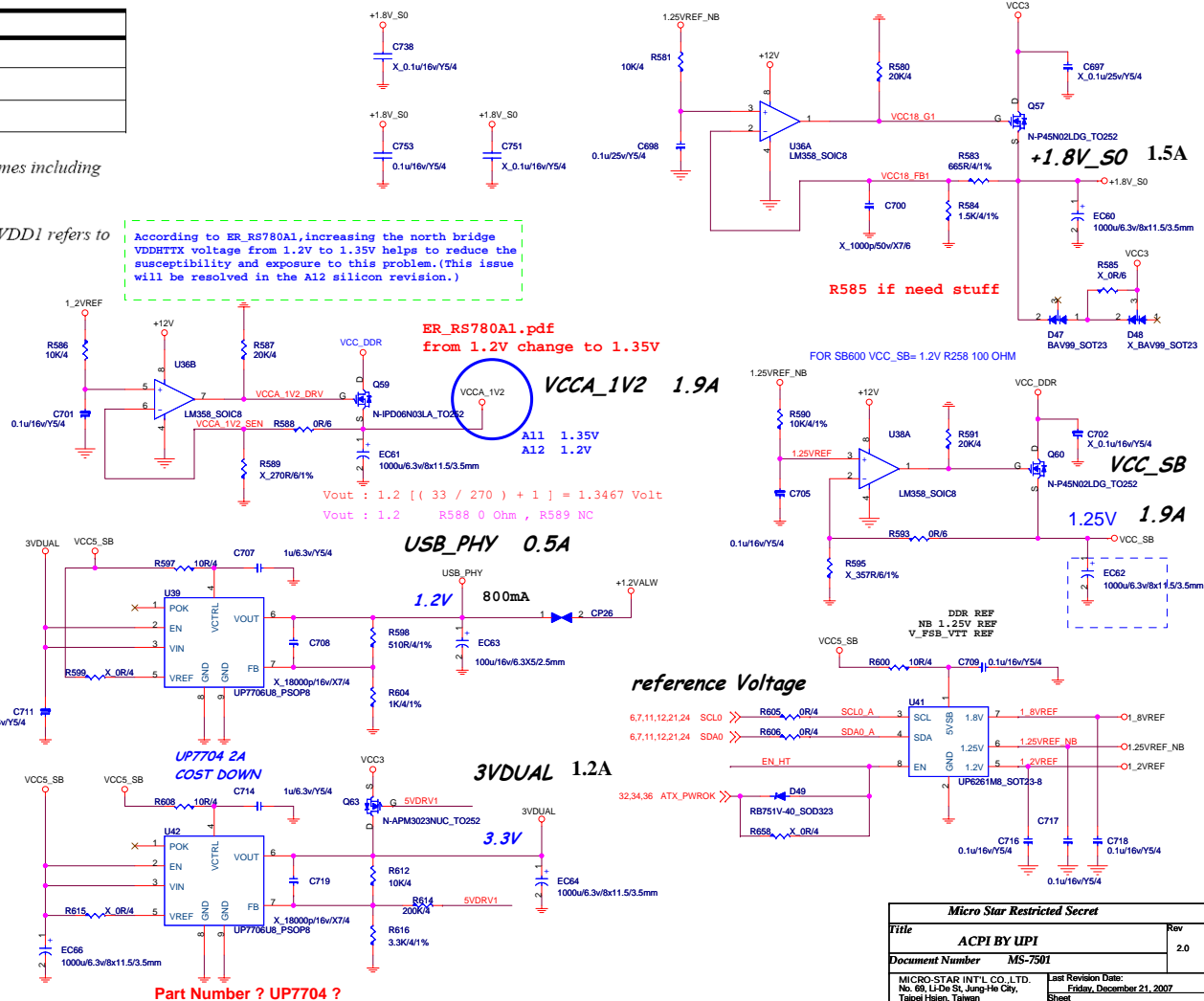
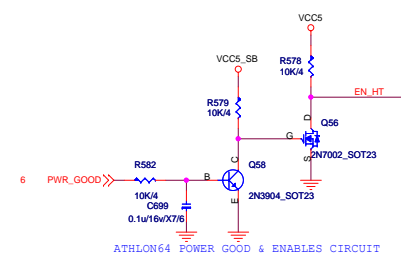
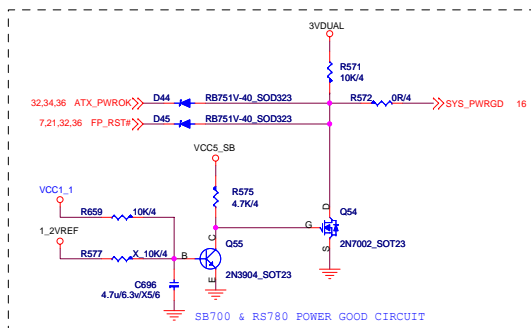
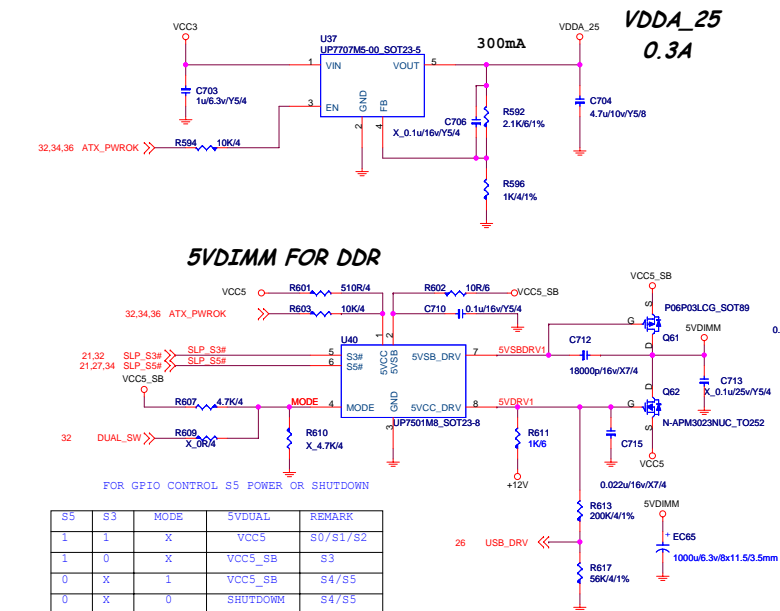
<b>Micro Star Restricted Secret</b>		
<b>Title</b>	<b>VCC_DDR &amp; VCC1_1 NB</b>	<b>Rev</b>
<b>Document Number</b>	<b>MS-7501</b>	<b>2.0</b>
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		<b>Last Revision Date:</b> Friday, December 21, 2007 <b>Sheet</b> 34 of 40

Table 15. Power Sequencing Group Definitions

Power Group A	Power Group B
VDDIO <sup>1,2</sup> <b>Vcc_DDR</b>	VDD[1:0] <sup>3</sup> <b>Vcore</b>
VTT <sup>1,2</sup> <b>VTT</b>	VDDNB <b>Vcore_NB</b>
VDDA <b>VDDA25</b>	VLDT <b>HT</b>

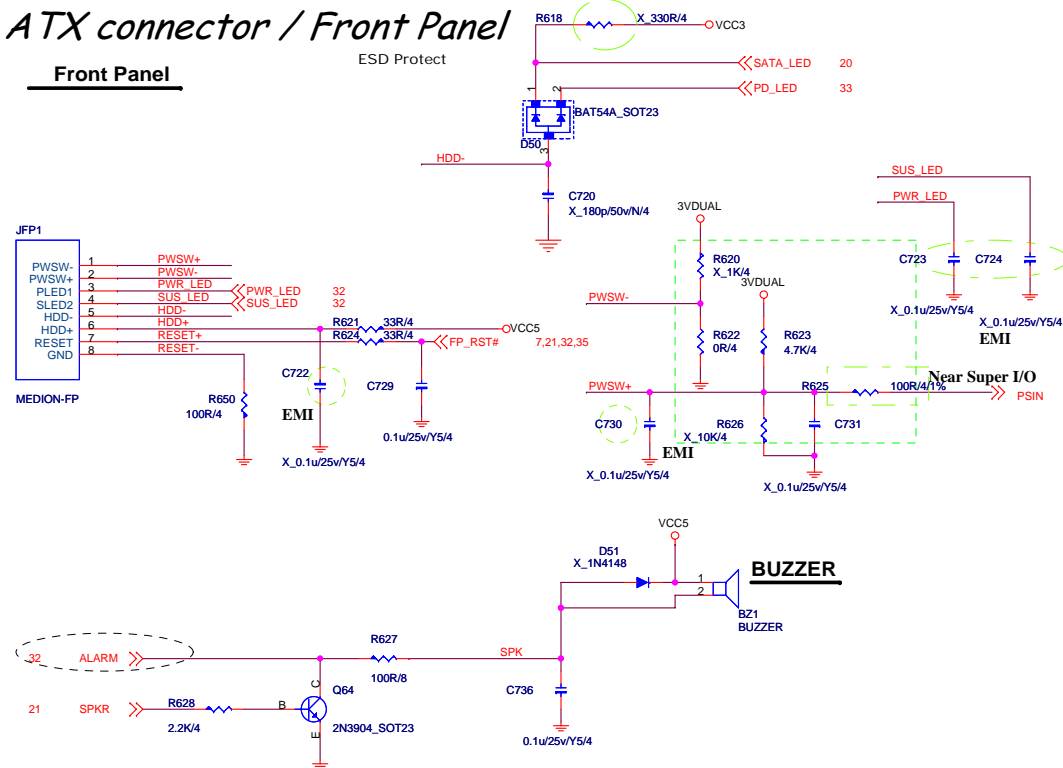
Notes:

- 1) VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.
- 2) VDDIO and VTT only apply to DDR2 compatible processors.
- 3) VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.

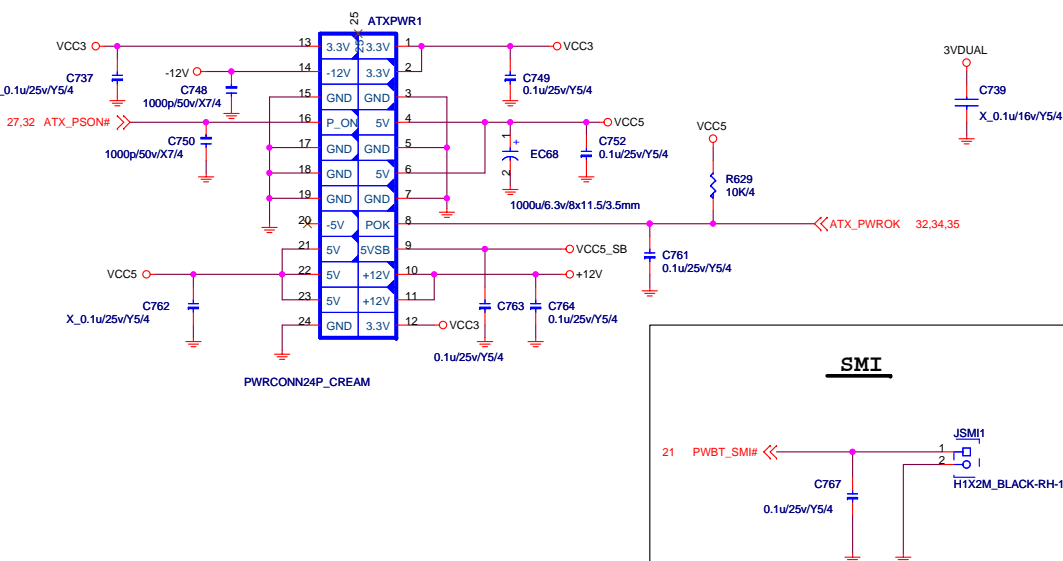


### ATX connector / Front Panel

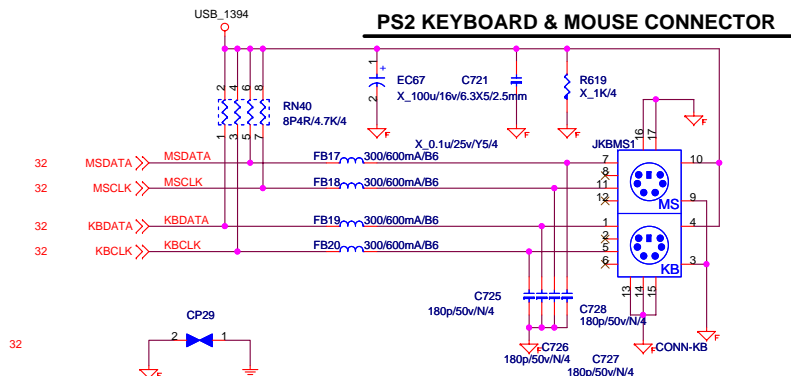
### Front Panel



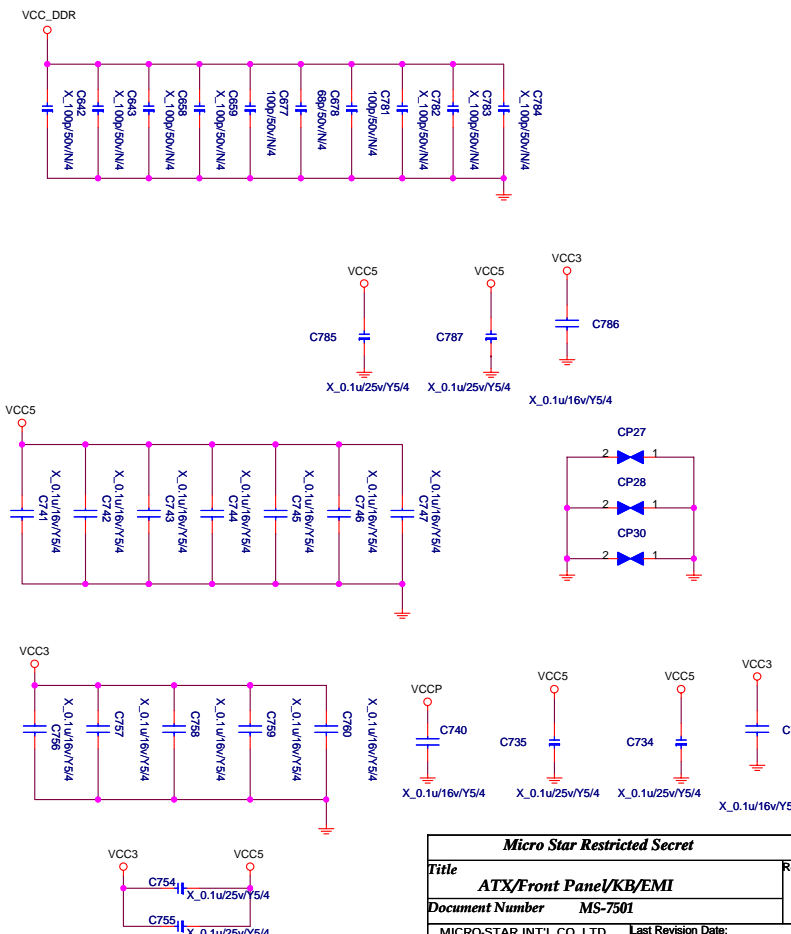
### ATX Connector



## PS2 KEYBOARD & MOUSE CONNECTOR

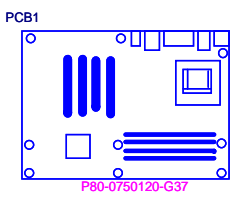


## EMI solution





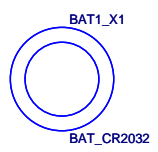
**PCB**



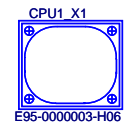
**PCB : 2116**

**P80-0750120-G37**  
**P80-0750120-E55**

**BATTERY**

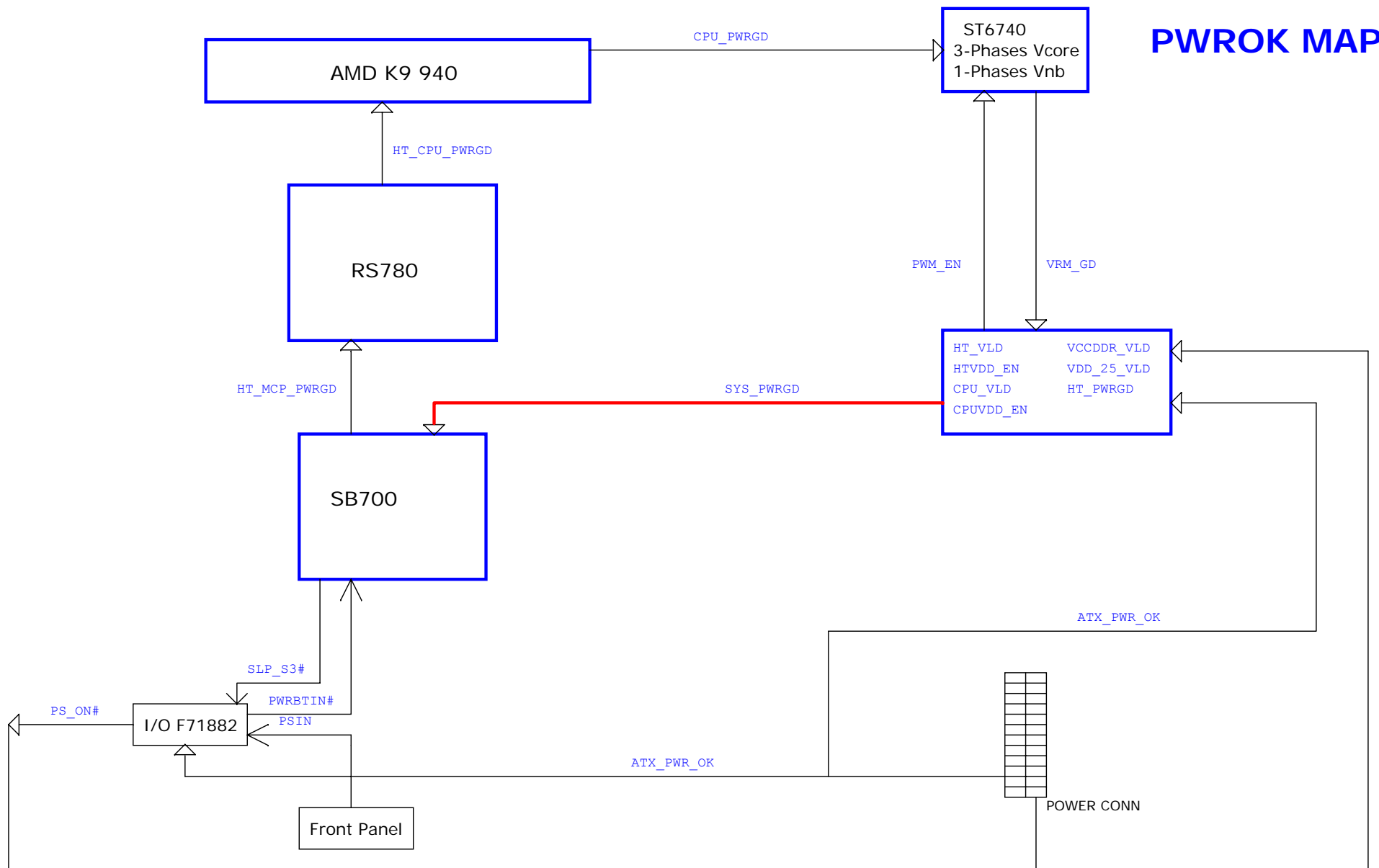


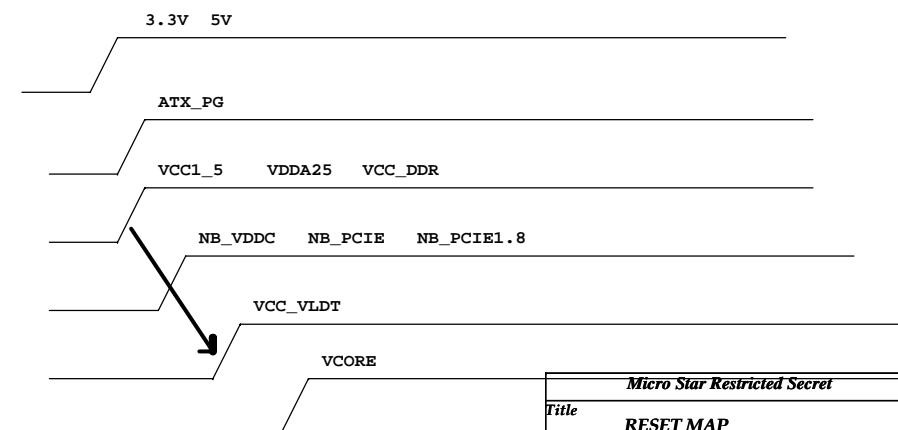
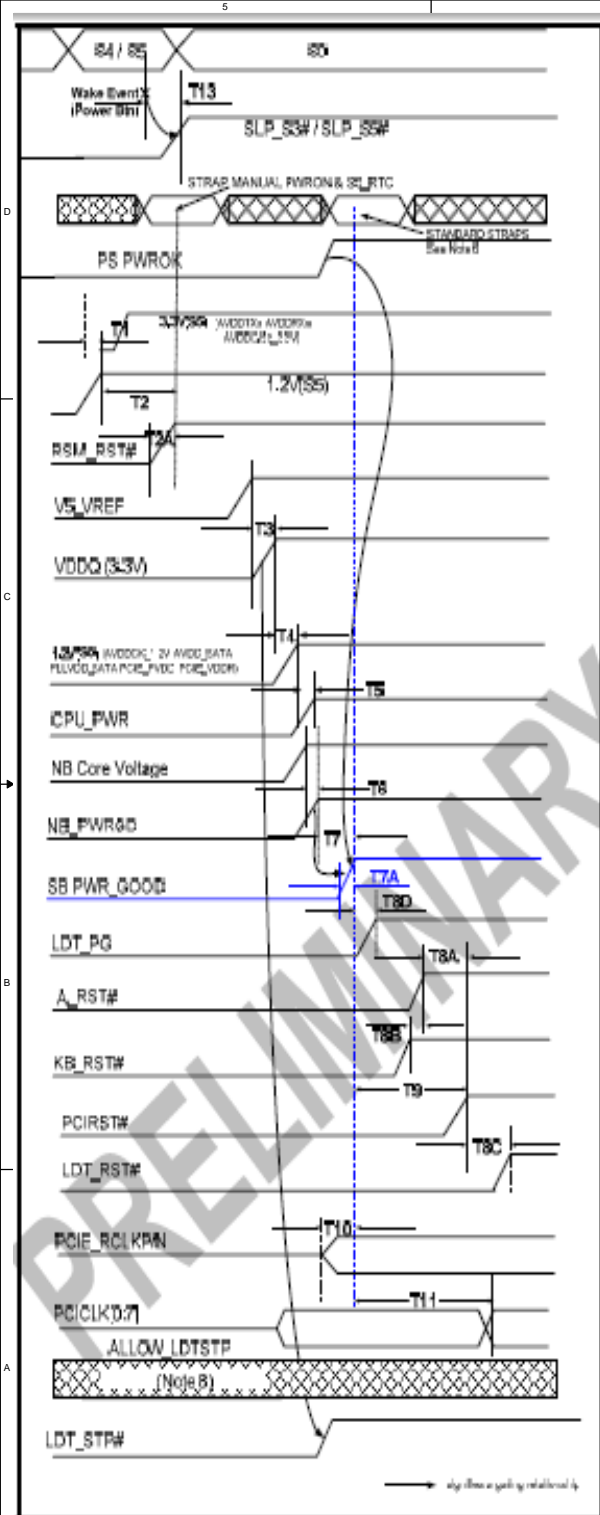
**CPU RM**



U10 & U13 new version ( Part number ) ?

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